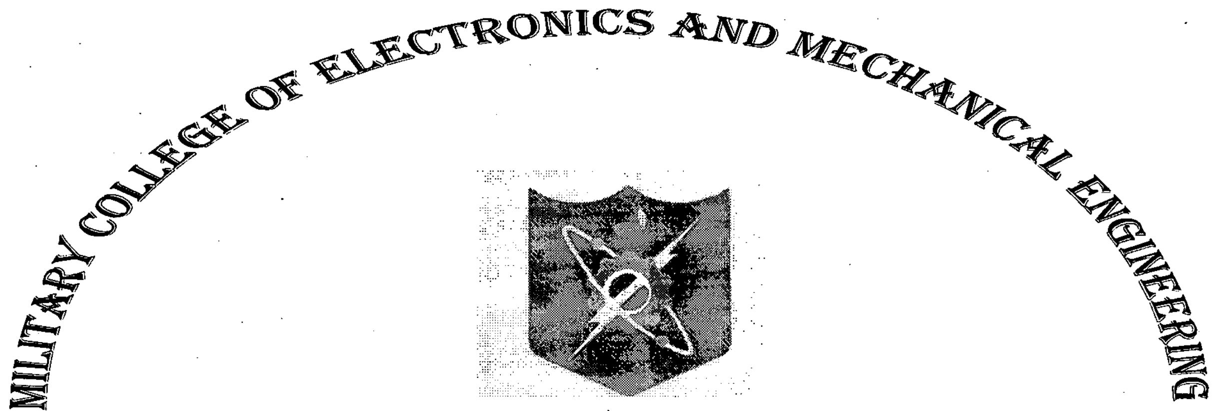

FACULTY OF ELECTRONICS

SECUNDERABAD

CERTIFICATE

Certified that this is a bonafide report of the dissertation work done by Major Ajay Malik during the year 1998 in partial fulfilment of the requirement for the award of the Degree of Master of Technology in Electrical Engineering by the Jawaharlal Nehru University, New Delhi.

External Examiner 21/7/98

Guide

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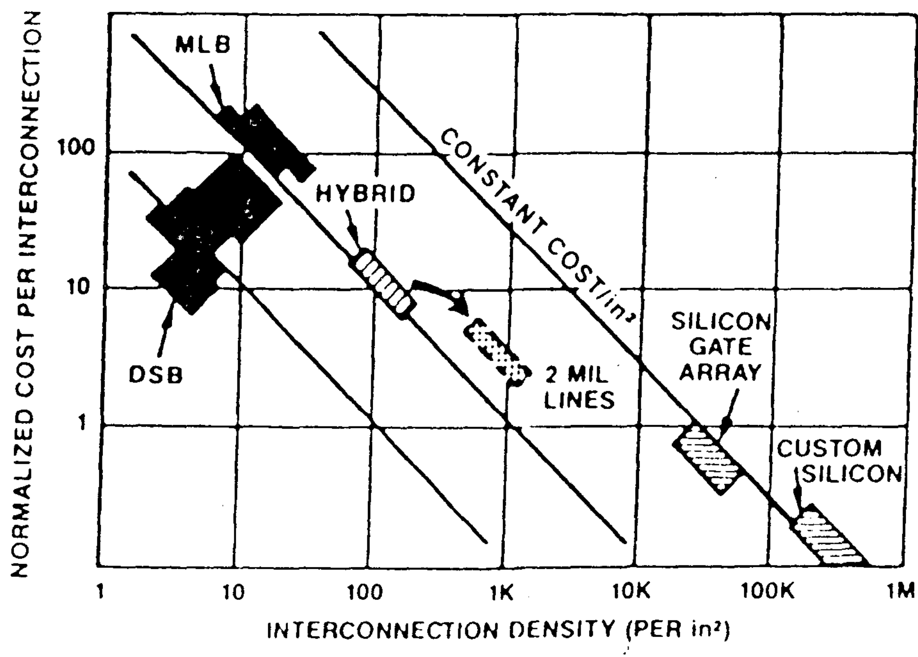
INTRODUCTION

1. Interconnection Systems. Advances in interconnection systems have occured in response to the evolution of electronic technology, particularly the growth in component sophistication, complexity, and number of electronic circuit component terminals to be interconnected. But a basic concern has developed with the progress of interconnection technology. A variety of factors have contributed to this growing concern, among which are the following :-

(a) Interconnection Costs. These have not followed the decline in device costs (Fig 1). Today a complete computer-on-a-chip costs less than the surrounding components and interconnection system.

(b) Operating Speeds. There is a strong trend towards increased use of the faster-operating integrated circuits (ICs). The interconnection system serving them should have configurations that make it possible to locate all such devices within a very limited area in order to avoid or minimize excessive propagation delays in the wiring.

(c) Integration of Functions. Further integration of circuit functions within dual-inline packages (DIPs) is becoming more limited, in part by the practical considerations of the economical size of the ICs and DIPs suitable for easy design change and field repair.



INTERCONNECTION COST VS DENSITY

FIGURE - 1

(d) **Lead Spacing**. Any increase in the number of leads per IC package calls for more interconnections between them (Table 1). Large-scale integrated circuits (LSIs) having from 48 up to 150 leads cannot be efficiently packaged in the familiar DIP configuration with two rows of leads on 0.1-inch centers. These devices will require the new packages that are coming onto the market.

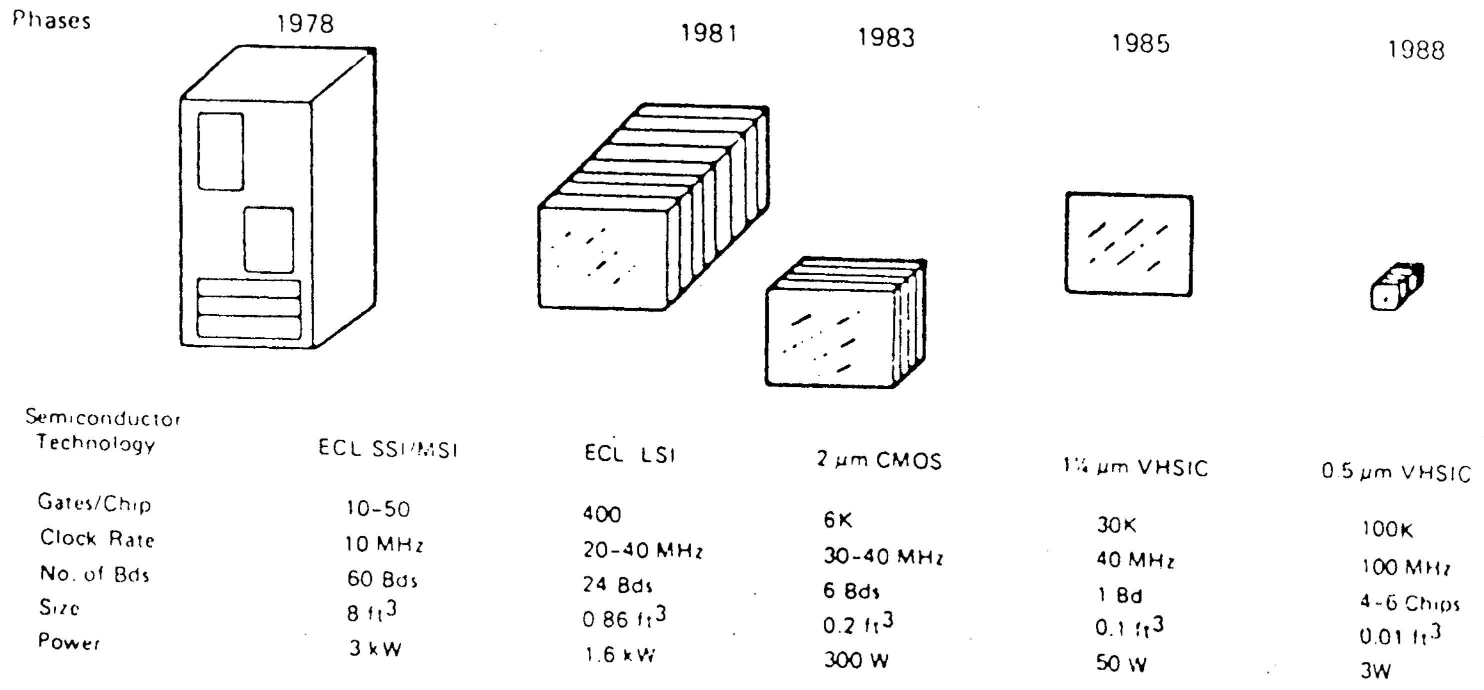
2. **Semiconductor Device Technology**. The application of the emerging higher-speed, higher-density ICs offers great potential for increasing the performance of complex electronic systems. This is especially true in applications where size, weight, and power requirements are critical. In order to fully utilize the potential of these new devices, compatible packaging technology is required. This demands a new definition of the interconnection system. The significance and magnitude of these new interconnection system requirements can be seen by appreciating the development of semiconductior technology (Fig 2).

3. As the semiconductors in electronic equipment go to the use of VLSI (Very Large Scale Integration), there will be a greater percentage of the total system cost, of the total design and manufacturing time, and of the testing costs affected by the packaging/interconnection system technology. Also, chip packaging levels will increase to over 10,000 gates/chip and board pinouts will approach 300, with proportional increases in power to be dissipated per unit volume. The use of peripheral devices such as DIPs and chip carriers, or matrix devices, such

TABLE 1

Connectivity Capacity Requirements for Dual-Inline Packages (DIPs) and Small Chip Carriers (Dimensions Only in Inches)

Case	Typical Packaging situation	Approximate number of pins per in.^{2}	Required connective capacity in./in^2	Wiring level		
				50-mil grid	25-mil grid	20-mil grid
1.	1-16 pin DIP per in.^{2}	15	34	2 (1.7)	1 (0.8)	1 (0.7)
2.	22-pin DIP on 1-in. centers	20	45	2.3 (2.3)	1+ (1.13)	1 (0.9)
3.	2-16 pin DIPs per in.^{2}	30	67	3-4 (3.4)	2 (1.68)	(1.34)
4.	40-pin DIP on 1-in. centers	20	45	2-3 (2.3)	1+ (1.13)	1 (0.9)
5.	24-pin chip carriers on 0.7 in. centers	50	112	~6 (5.6)	~3 (2.8)	~3 (2.2)
6.	24-pin chip carriers on 0.5-in. centers	16	216	~11 (10.8)	~6 (5.4)	~5 (4.3)
	Connective capacity per level, in./in^2			20	40	50



SEMICONDUCTOR TECHNOLOGY DEVELOPMENT

FIGURE - 2

as pin-grid arrays, will significantly affect packaging density and therefore, the interconnection system.

4. <u>Surface Mounting</u>. Present component interconnection technology is based to a great extent on the use of plated-through holes, and therefore all devices or their packages must have leads that will be eventually soldered into these holes. These component leads add to material costs, assembly labour, and manufacturing problems, but they are conceptually totally avoidable.

5. The newly emerging packages are radically resolving this problem, since they are designed for the surface mounting of planar components on a planar surface and do not require discrete component leads and plated-through holes for their termination. This development will have a profound impact on future interconnection methods, because the surface-attachment approach achieves the following :-

(a) Eliminates the cost and labour for component leads and their forming.

(b) Simplifies the problems of component shipping and handling by the elimination of their delicate leads.

(c) Simplifies assembly, since there are no leads to preform. Also, the self-centering capability of many of these new devices during the soldering operation makes them tolerant to some component placement misalignment.

(d) Increases the component placement rate from 300 units/hour (for manual assembly) or 3,000 or more units/hour (for automated methods) by one more order of magnitude, e.g., 200 units in 7 sec on an 8- by 10-in. board is achievable.

(e) Simplifies the soldering process by assembling with solder-reflow systems that use vapor-condensation methods without the need to worry about leads protruding on the underside of the substrate.

(f) Improves connectivity/unit area on the underlying substrate by reducing hole diameters, or by totally eliminating the need for holes.

6. <u>**Summary**</u>. Microelectronics has revolutionized the architecture and design concepts of the present day products. Every two or three years a new technology generation is announced. 1991 saw the breakthrough of a feature size of 0.8 micron for CMOS and 1992 saw that of 0.5 micron. Most developments are using three interconnection layers as a tripple layer metallization will be mandatory for 0.5 micron technologies because interconnection delays have become more significant than gate delays. It is therefore time that due consideration is given to surface mount and chip on board technologies for optimizing the chip space.

SEMICONDUCTOR DEVELOPMENTS

General

7. Much has been written about Surface Mount Technology (SMT) and how, in general terms, it better satisfies the growing demand for packaging and interconnecting high-technology integrated ccts, than does conventional through-hole technology. However, now that an SMT state-of-art is beginning to emerge, this is an appropriate time to become more specific about the new developments in semiconductor technology that are driving force behind SMT and, thereby, behind printed board technology.

8. During the last few years, the number of approaches available to cct designers to use (or create) integrated ccts has blossomed into a wide variety (Table 2). Therefore, an endeavour is made to first describes the standard semiconductor logic and the sophisticated custom/semicustom ways in which they are being combined by integrated cct (IC) manufacturers and this is followed by a discussion of how this impacts end-product applications. Finally, their ultimate impact on surface mount-related issues is covered.

9. Integrated Circuit Logic Families. A cct designer can work with one of several integrated cct transistor structures. The two most popular are bipolar and metal oxide (MOS) silicon chip technologies. These, in turn, are beginning to receive competition from the newly emerging gallium arsenide (GaAs) chip structures.

TABLE 2

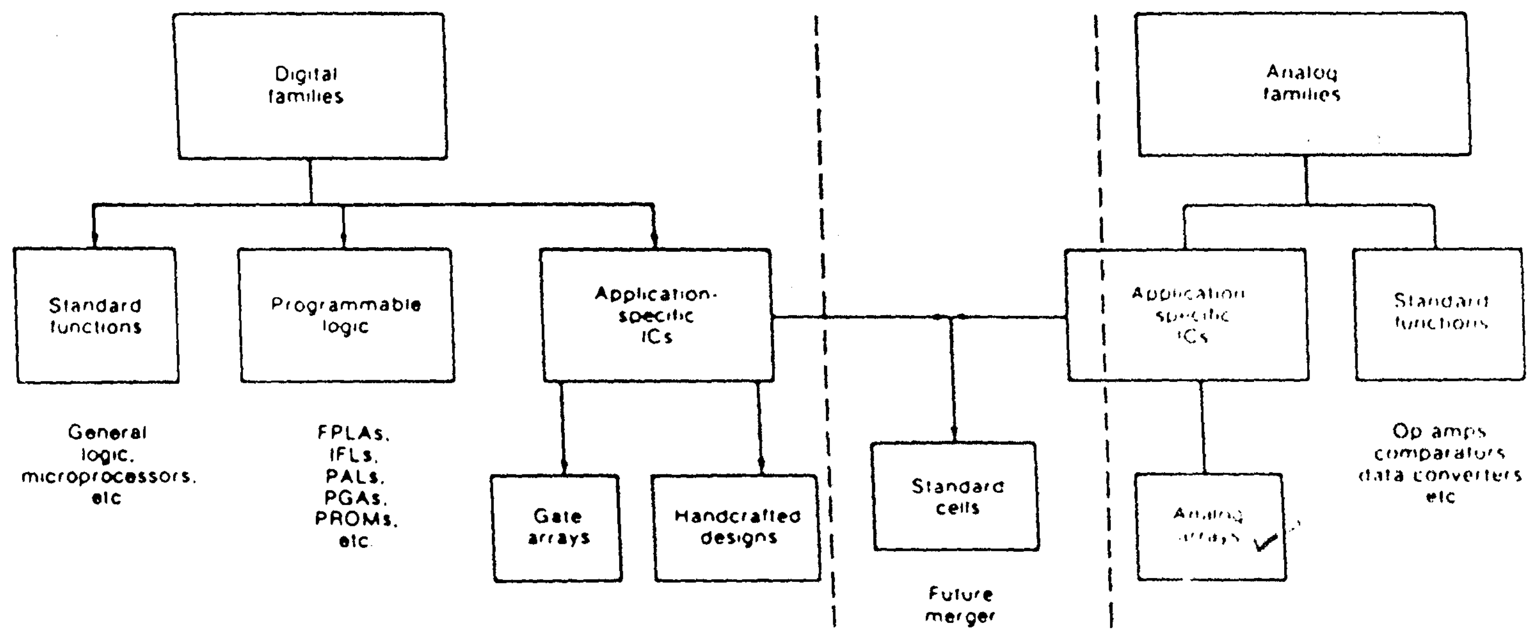
Examples of High Speed Integrated Circuits [7]

	GaAs	ECL	CMOS
Critical dimensions (Micro meter)	1.0	2.0	2.0
Chip size (mm^2)	4.6 x 4.3	6.6 x 6.8	10 x 10
No of equivalent gates	1200	2500	20K
Time delay (psec/gate)	375	510	1500
Power dissipation (Micro Watt/gate) (50-MHz clock)	190	1200	310
Speed-Power (f)	71	610	465

10. The demise of the standard silicon-based logic families has been forecast for almost as long as standard logic has been around. And true, the standard logic families that exist today are a far cry from those of the 1960s. Yet their use persists. Simple one- and two-gate chips are gradually being made obsolete by standard medium-scale integration (MSI) and in some cases, by large-scale integration (LSI) chips with larger functions. However, the most basic building block functions will remain as extra "glue" circuits for many years to come.

11. Gate-switching speed, power dissipation, and functional density are the basic differences separating the integrated circuit technologies at the low-integration levels (Fig 3). However, these are no longer valid in the very-large-scale integration (VLSI) era. Thus, the answers to selection questions lie in understanding the available technologies from the new perspective of identifying the applications areas most generally suited for each technology and the key system design trade-offs involved in the use of each technology.

12. <u>Bipolar Circuit Technolgy</u>. Bipolar transistors can be formed by either alloy or double-diffused techniques. However, all major bipolar "integrated" ccts use double-diffused transistors formed in an epitaxial (high-resistivity film) layer deposited on the silicon wafer. The epitaxial layer serves as the "collector" region of the transistor and allows for easy isolation of the separate cct components with the addition of a deep diffused "fence". Because they are formed below the wafer surface, bipolar



WIDE VARIETY OF INTEGRATED CIRCUIT TECHNOLOGIES

FIGURE - 3

transistor are not prone to contamination. Unsensitivity to contamination is not the only factor, however, they can operate at voltage and current values that are compatible with other electrical devices. The switching speeds of bipolar transistors are also faster than those of the simpler MOS discrete transistors.

13. Using conventional bipolar structures, cct speed can be improved by "wiring" together the various elements into logic cells. Transistor-transistor logic (TTL) and emitter-coupled logic (ECL) are the two most popular cell types.

14. TTL ccts have been popular with most system builders because of a combination of acceptable performance and ease of design. Alternately, ECL design has been a standard process only for computer builders who need high performance badly enough to put up with the special headaches by the use of the higher-speed ECL ccts. For example, printed board conductors must be designed with wave guide (controlled impedance) techniques because the rise time of ECL signals puts them in the microwave freq range. This point will be discussed in greater details subsequently.

15. <u>MOS Circuit Technology</u>. The formation of MOS integrated cct devices is different from bipolar technology. The basic MOS fabrication process starts with an incoming wafer that is processsed through oxidation and goes directly to masking. Thus, it can eliminate the epitaxial layer and isolation diffusion steps reqd in bipolar technology. The absence of the isolation

structure allows a higher MOS component density than bipolar technology.

16. In both bipolar and MOS technology, the area of the cct that does not contain active devices is called the "field". A particular problem arises over the field in MOS ccts. Metal conductors running on top of the field oxide form a capacitor with the silicon below. If the voltage on the conductors becomes high enough, the "field capacitor " will create charge in the underlying silicon and cause shorted devices. Additional wafer processing is reqd to overcome this problem. (More careful handling during the printed board assembly processs is also reqd).

17. Unlike the simpler metal gate processing, complementary MOS (CMOS) requires more processing steps than the biploar process. However, this additional processing results in CMOS devices that have lower power comsumption and increased speed, making them attractive for many applications.

18. The Departments of Defence of all the countries and the aerospace industry have stepped up their requirements for increasingly higher tolerances against radiation effects for integrated ccts. These stricter mandates are expected to yield greater system survivability in hostile (nuclear) environments. Bipolar technology is inherently more radiation-resistant than most CMOS processes. Thus, the advantages of designing with CMOS have led to additional processing steps to enhance CMOS survivability. Other CMOS processing variations prevail to

customize particular features of the end product. This, in many cases, makes CMOS the most complicated and most involved technology in the industry.

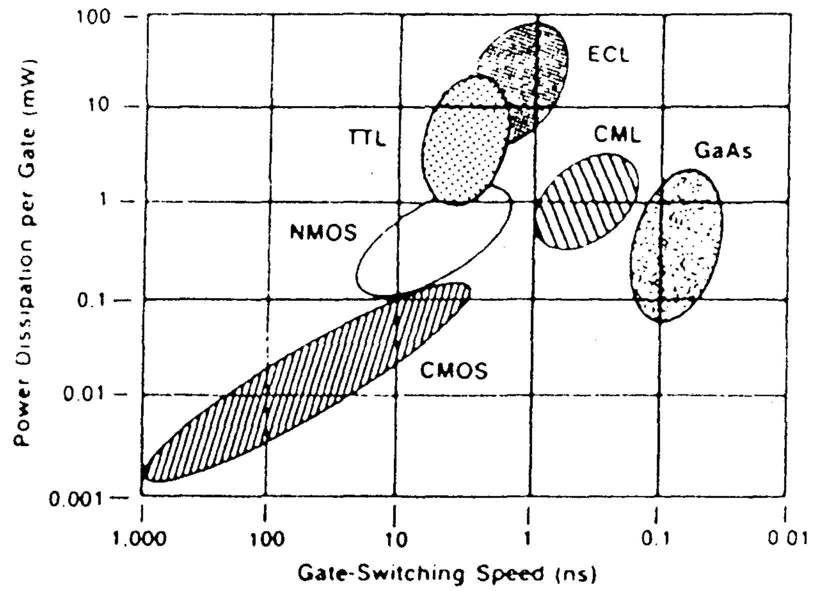
19. **Gallium Arsenide Technology**. Gallium arsenide (GaAs) is an ideal semiconductor medium for achieving very high speed in electronic devices and integrated ccts. This is because its energy band structure is such that electrons in GaAs are exceedingly "light" and highly mobile. Thus, electron velocities measured in GaAs transistor structures range upto about five times those achieved in silicon-based devices.

20. Further more, GaAs is readily available in a semi-insulating substrate form that substantially reduces parasitic capacitances, so that its outstanding device speeds can be fully realized in integrated ccts (Fig 4). This high speed, plus power dissipation that often tends to be substantially lower than that of high-speed silicon devices, accounts for the growing interest in gallium arsenide.

21. Although a number of different GaAs integrated circuit families exist, it is possible to draw some general conclusions about the advantages of GaAs technology over silicon technology.

22. Currently, for the same power consumption, GaAs is about half an order of magnitude faster than emitter-coupled logic (ECL), the fastest silicon-based family.

(a) GaAs is more radiation-hard than silicon. At this time, however, the difference is difficult to quantify.



SPEED VS POWER COMPARISONS FOR VARIOUS TECHNOLOGIES.

FIGURE-4

(b) GaAs is better suited to the efficient integration of electronic and optic components. The usefulness of GaAs for this type of integration is still under investigation. However, if developed to the appropriate level, this may have a major impact on system design in general.

23. Basic disadvantages of GaAs technology, as compared to silicon technology, are as follows :-

(a) GaAs wafers presently exhibit a large "density of dislocations". That is to say, there are a large number of irregularities per unit area. Consequently, GaAs chips have (military writing) :-

(i) To be smaller in area.

(ii) A smaller transistor count.

(iii) A poorer yield. Of course, chip size can be traded off against production yield to some extent.

(b) GaAs substrates are about two times more expensive than silicon substrates. Moreover, GaAs is brittle Wafers can be damaged easily during the fabrication of intergrated circuits.

(c) The noise margin of GaAs at present is not as good as that of silicon. Thus, it is often necessary to trade off chip area for higher reliability.

(d) Lastly, some companies are currently reporting problems with the testing of designs for high-speed GaAs integrated

circuits. Testing facilities that are fast enough are simply not yet available. But this situation is expected to improve.

24. Application Specific Integrated Circuits. Electronic system design is becoming more complex, with architectures reaching new heights of sophistication and expanding integrated circuit choices. Yesterday's systems comprised off-the-shelf, small-scale (SSI) and medium-scale (MSI) levels of circuit integration. However, many of today's designs are implemented with customized large-scale (LSI) and very-large-scale (VLSI) integration. Leading the migration toward LSI/VLSI are applicaion-specific integrated circuits (ASICs) with functions tailored to the user's requirements.

25. Therefore, in order to keep their competitive edge, system manufacturers must make informed decisions when slecting a particular type of customized integrated circuit technology. This often requires an in-depth trade-off analysis.

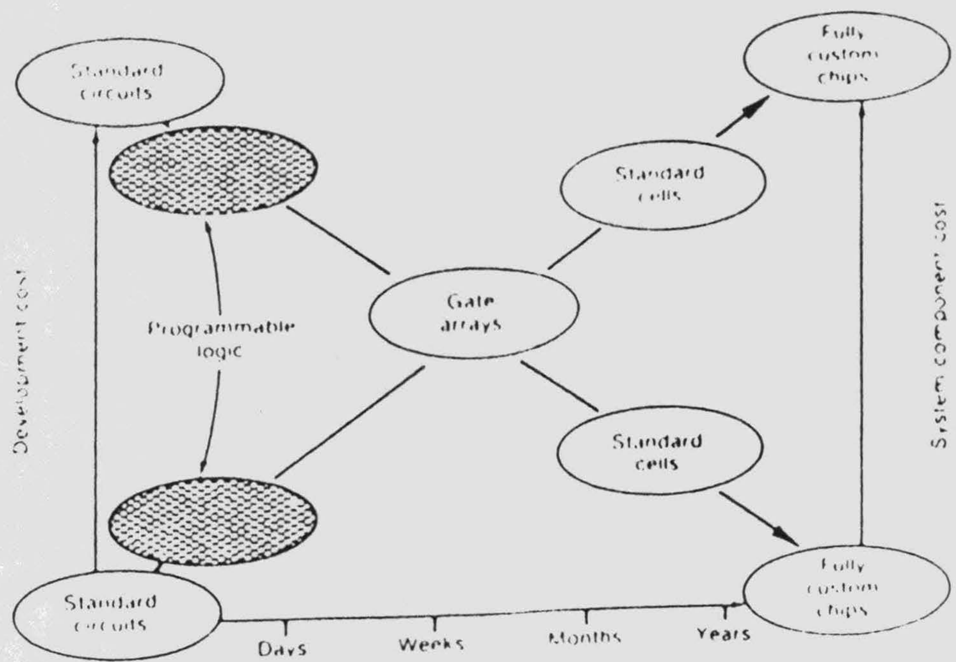
26. There are four general ASIC categories :-

(a) Programmable Logic Devices (PLDs).

(b) Gate/macrocell arrays.

(c) Cell-based devices (both standard/macrosystem cells and silicon-compiled cells).

(d) Handcrafted, fully custom integrated circuits (Fig 5). The gate arrays and cell-based devices are often called semicustom integrated circuits. Also, recent advances in



INTEGRATED CIRCUIT DEVELOPMENTS : TIME VS COST

FIGURE-5

TABLE 3 ✓

ASIC Technology Selection Factors

	ASIC types			
	Programmable, logic	Gate/macrocell arrays	Standard Cell/ macro systems	Handpacked custom
Chip density (number of gates)	Few	16-100,000	Hundreds to tens of thousands	From hundreds to tens of thousands
Percent of wafer pre-processed	100	80-90	0	0
Time to prototypes (weeks, in 1983)	Off-the-Shelf	7-13	13-26	39-104
Option development cost per chip (depends on complexity)	None	$10,000-$40,000	$40,000-$100,000	$100,000-$500,000
Ability to make design changes or correction	Minimal cost	Easy, fast, and expensive	Easy, but somewhat more expensive and slower than arrays	Hard, slower, and more than standard cell/macrosystems
Unit production cost of chip	Low	High	Medium	Lowest

ASIC = Application Specific IC

integrated circuit fabrication are spawning a new kind of ASIC between a PLD and a gate array. It is important to determine which type is best suited to a designer's requirements (Table 3). The first consideration is the density of the device needed. For example, PLDs have relatively low densities of from 50 to 5000 equivalent gates per chip.

27. Macrocell and gate arrays are next, with densities ranging from 500 to 10,000 gates per chip, sometimes more for specific purposes. Standard cells have still higher densities, many thousands of equivalent gates per chip. Hand-packed custom circuits are the densest, with 70,000 switching transistors per chip being not uncommon.

28. The time to prototype and develop an ASIC is best suited for an application. Because PLDs are readily available off the shelf, prototypes can be obtained almost immediately at a relatively negligible development cost. Gate array and macrocell array prototypes development time is typically from 7 to 13 weeks, with prototype costs from $10,000 to $40,000. Standard cells take even longer, typically from 13 to 26 weeks, because their wafers are made from scratch instead of being preprocessed like macrocell and gate array chip.

29. Additionally, standard-cell prototyping costs are usually between $40,000 and $100,000. Handpacked, fully custom chips have the longest prototyping times, taking from 39 weeks to 2 years, with costs ranging from $100,000 to more than $50,000.

30. PLDs are often the logical choice when the product is required immediately or when frequent design changes are to occur. They are limited, though, to relatively simple requirements when compared to the functionality and densities of the other ASIC technologies. Its functional and volume requirements are high, gate array and macrocell solutions are usually the most feasible, with standard cell circuits the choice for the highest-volume demands. However, the better silicon usage characteristics of standard cells may offset their higher development costs if the volumes are suitable.

31. Silicon-compiled ASICs, though still in their infancy, also deserve consideration. Handpacked, custom circuits are often acceptable when the largest production quantities are needed and if the long turnaround time can be tolerated by the user.

32. Programmable Logic Devices. Until recently, programmable logic devices (PLDs) were considered for use primarily as TTL "glue" replacements in order to compact several gates into a single package when there were shortages in printed board space. They were not really accepted as a valid ASIC choice. But that has changed, due to four basic reasons :-

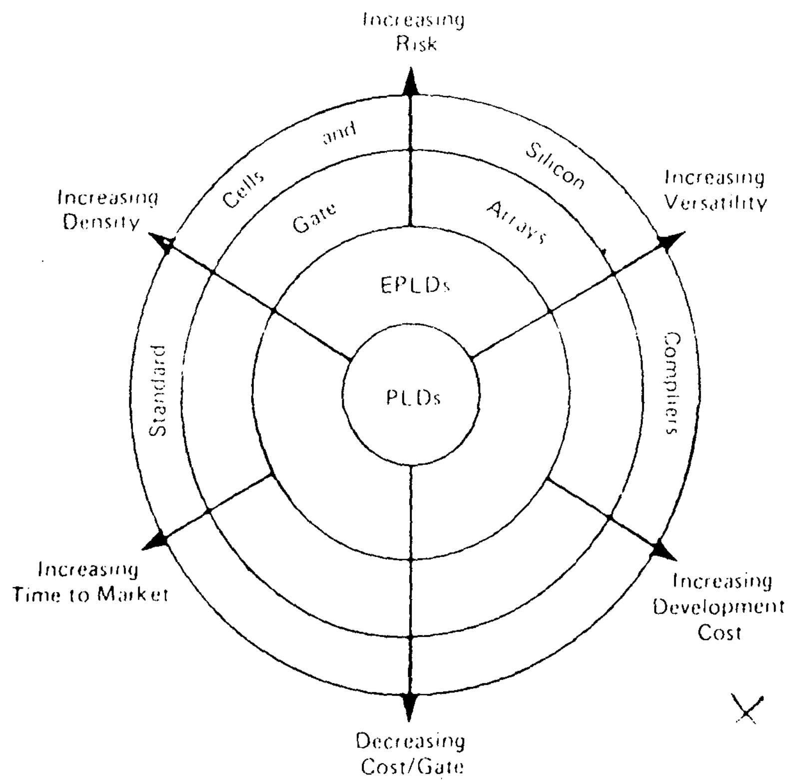
(a) The first is the trend toward acceptance of PLDs as a mainstream system building block, such that the designer begins a design with PLDs in mind, as opposed to their being an afterthought.

(b) The second reason is the sudden proliferation of PLD manufacturing technologies. Just as digital logic gates began with bipolar chips, so did PLDs. Now, however, PLDs are available in a selection that also includes CMOS and ECL technologies.

(c) Third is the growth in the complexity and functionality of PLDs. Early PLDs (in-20-pin, dual-inline packages, DIPs) had usable gate conunts in the 100- to 300-gate range. Now, gate densities have climbed to as high as a few thousand. (Pin counts have also increased to as high as 84). The result is that such devices now offer logic densities that once were the exclusive domain of gate arrays and cell-based parts.

(d) The fourth reason is the increase of PLD manufacturers, from three in 1979 to more than 20 today. This has served both to increase the selection of functions available to the designer and to make the cost of the devices more competitive.

Applying CMOS and erasable-cell technologies to the basic D configuration has created erasable programmable logic devices PLDs) with a new level of versatility in logic design. In rtain applications they match the density of gate arrays thout the associated tooling costs, extended development hedules, and loss of in-house design control. Thus, EPLDs fit tween PLDs and gate arrays in terms of complexity, versatility, d cost per function (Fig 6).



TRADE OFFS WHILE SPECIFYING ASIC TECHNOLOGY

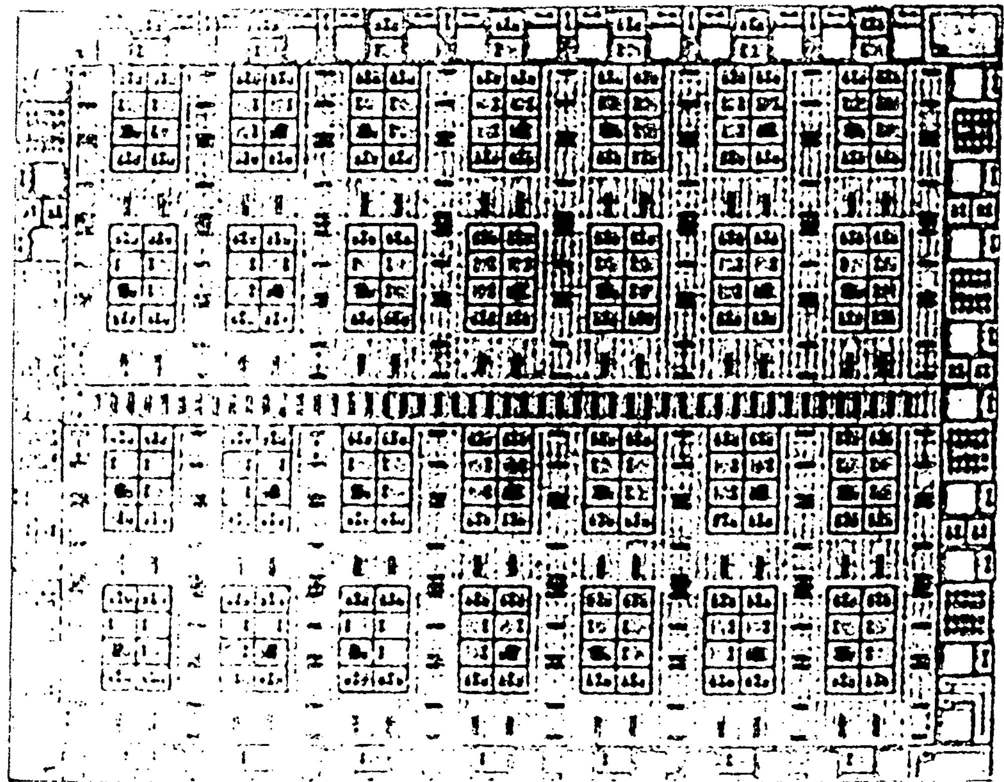
FIGURE -6

34. **Gate Arrays.** Gate arrays are distinguished by their use of prefabricated chips containing transistors and "feedthroughs," none of which are interconnected by signal wiring (Fig 7). As a result, the chip vendor can make large quantities of identical unwired gate array chips, fabricating the wiring only when a customer supplies the circuit schematics or interconnect lists.

35. Since the fabrication of wiring layers is a relatively low-risk, in-expensive operation, manufacturing yields tend to be high and processing times short. More important, design costs are low, since a manual layout phase is not needed.

36. Instead, design automation tools, which assign transistors and feedthroughs to circuit functions and determine the wiring paths, perform the layout task. The use of these tools is straightforward, consumes a relatively small amount of computational resources, and tends to produce final chips that are efficient in space and speed.

37. Arrays are available in all of, and combinations of, the basic integrated circuit fabrication technoligies. The mainstay of the fastest digital systems, silicon ECL gate arrays, face competition from the other technologies as new processes and materials become available. However, the same technological advances that give MOS its advantages will help bipolar arrays remain ahead of MOS as well as mixed bipolar-MOS and in stride with the subnanosecond speeds of gallium arsenide. In fact, ECL gate arrays will soon be available with as many as 10,000 gates along with gate delays of only 200 to 300 psec.



BIPOLAR 28 ARRAY INTEGRATED CIRCUIT (GATE ARRAY)

FIGURE - 7

38. Nonetheless, ECL does stand to lose its edge in certain fields. For instance, printed boards built previously with SSI and MSI ECL chips can now be replaced by high-density CMOS gate arrays and mixed bipolar-CMOS chips with delys of several hundred picseconds and integration levels of 20,000 gates and higher. At the same time, GaAs may outrun ECL in some designs calling for extremely high speed. GaAs logic arrays and standard cells now have delays of only 200 psec or less with complexities up to a few thousand gates (Table 4).

39. **Cell-Based Technology**. Cell-based ASICs can be implemented either as standard cells or as compiled cells. Both technologies provide high levels of integration, flexibility, and performance. The trade-offs are in degree of user involvement and functional capability.

40. Turnaround time and nonrecurring engineering costs are similar for the two approaches. However, designing with standard cells relinquishes more of the design effort to the device vendor than does the compiled-cell approach, which allows the customer to be more involved. Also, although the performance of standard and compiled cells may be the same at the transistor level, performance and density differences emerge at the chip level (Table 5).

41. It should be noted, however, that neither approach is inherently superior or preferable to the other. Rather, the decision to use one or the other depends on the application or parts of the application. For example, some on-chip memory is

TABLE 4

Typical State-of-the Art Gate Arrays

	Number of gates	Gate delays	Package Pins	Number I/Os
Bipolar gate array	8,000	210 psec	235 PGA	188
CMOS gate array	20,000	400 psec	284 TAB or PGA	238
GaAs gate array	2,000	230 psec	88 LCC	80

TABLE 5

Three Implementations of the Same Circuit

	Cell Compiler	Standard Cell	Gate array
Core size	1085 x 1112	1872 x 1740	2160 x 2112
Number of transistors in core	980	1286	1286
Transistor density (sq.mils per transistor)	1.91	3.93	5.49
Design time	4 days	7 days	7 days
Performance (critical path delay per gate)	45 nsec	68 nsec	49 nsec[a]

a - The gate array design is implemented in a faster CMOS process technology.

more easily implemented using comilers, while many logic functions are better implemented in standard cells. A few vendors even provide the ability to implement both approaches on the same chip for optimum flexibility.

42. A Standard cell uses a library of simple, fixed cells and soft macrocells (predefined combinations of cells). User involvement typically includes logic partitioning, schematic entry, simulation, and net list verification. Fixed-height cells are then arranged by automatic placement and routing programs in fixed-height rows separated by variable-width routing channels.

43. Standard cell placement and routing is usually handled by the device vendor rather than by the customer. After the place-and-route operation, the design is resimulated using actual wiring delay figures to help ensure accurate performance estimation.

44. A cell compiler is a design tool for automatically generating the layout, simulation models, and schematic symbols targeted for a specific function. However, since one compiler cannot generate layouts for all functions, a design environment usually includes a libarary of cell compilers or parameter-based software modules.

45. In concept, a system engineer can design a chip by identifying compiler functions that correspond to the block diagram description of a circuit. These functions are compiled by the software. The design process then proceeds in a manner that is similar to that for standard cells.

46. <u>Fully Customised (Handcrafted) Devices</u>. A fully customised device imples that little or no formality is exploited in easing the task of chip design. For VLSI circuits, custom design uses heirarchical design methods whereby the bottom-most design element or cell contains the basic circuits, much like cells in standard cell devices. The primary difference is that there is little or no predefined structure to a custom-designed cell.

47. These cells are then interconnected to form larger cells, which are interconnected to form still larger cells, and so on until the entire chip is completed. The cells are not constrained into predetermined rows but can be located anywhere on the chip to minimize wasted space. A typical custom-designed chip is shown in Fig 7.

48. Cell placement and net routing in a custom layout are complex tasks, especially if maximum cell packing is desired. Because regular channels for wiring are usually not created, the task of routing is less constrained than in channel routing.

49. Even in a custom layout, however, routing can be done in two steps. The first step, as in gate array and standard cell designs, is to assign nets to particular regions of the chip or channels, if all cells are rectilinerar. Then each region is routed by assigned routes to tracks.

50. Cell placement on a custom chip is similar to the procedure for standard cell chips. Again, as in the standard cell approach, the object is to minimize wiring length and

congestion, assuring 100% wireability, and to minimize the area used by cells on the chip.

51. Custom design and layout, the most time-consuming of the ASIC styles discussed in this chapter, produce the most area-efficient chips and usually the fastest circuits. The trade-offs are with respect to design time, performance, chip size, production yield, and costs (both component and system).

52. **Specialised Technology**. In addition to the state-of-the-art integrated circuit technologies and architectures just described, other, more specialized approaches are being undertaken to obtain more cost-effective performance than is presently possible. Efforts in these areas are either vendor-driven (wafer-scale integration, silicon-on-sapphire, bubble memories, etc.) or user-driven (e.g., very-high-speed integrated circuits). Although in their relative infancy, developments in these technologies have a potentially great impact on printed board technology.

53. **Wafer-Scale Integration**. Wafer-scale integration (WSI) is conceptually the ability to interconnect electrically sound circuits on a tested and mapped semiconductior wafer using a wafer-level interconnect scheme. If achieved, WSI could open a market with almost limitless application. After nearly two decades of effort by several companies, however, a number of problems still exist (particularly in the wiring approach) that make these devices irrepairable, expensive, and, in general, unsuited to volume production. But because the benefits of WSI

are so alluring, new companies (and approaches) have emerged to address the issues associated with this challenging integration concept.

54. Attempts so far to implement wafer-scale parts have concentrated on integrating highly complex devices with a random point-to-point wafer-level interconnect. Although integrating such devices will eventually result in wafer-level products with performance characteristics equivalent to a mainframe computer, testing the viability of such complex devices may be overly optimistic for such an immature technology. Integrating less complex, higher-yield circuits in a more structured or bus-oriented architecture might be a more realistic endeavour.

55. Memory devices are the most logical and likely candidates to usher in this new generation of WSI system designs. For one thing, memory devices, in general are bus-oriented. This makes routing less complex and less prone to error. Also, memory circuits are often constructed with a single layer of metallization, allowing the multichip macrocircuits to be interconnected with a second layer (this type of double-layer metallization is a commonly used fabrication technology). One of the most likely candidates for a WSI memory device is in airborne- or satellite-based electronics that would benefit from the decreased size and weight that WSI memory devices could provide along with reduced power supply costs, lower cooling costs, and improved space optimization.

56. Conversely, there are studies that indicate that WSI is not practical for most applications. For example, there are those who feel that existing advanced VLSI-hybrid packaging approaches can achieve circuit density, performace, and cost-effectiveness levels comparable to those that WSI potentially possesses (Table 6). It is also claimed that, in terms of packaging density, thin-film multilayer hybrid circuits on varius substrates, when populated on both sides, can package almost 25% to 30% more components in about the same area as a wafer-scale device. The two technologies are almost equal as far as package delay concerned. (Double-sided thin-film hybrids rate 10.5-nsec versus 11.8-nsec for WSI when both have 450 output buffers per package).

57. In terms of power per chip, both single- and double-sided multilayer hybrid approaches are competitive with WSI. When the product of power times delay (an accepted figure-of-merit used to compare such technologies) is considered, double-sided thin-film hybrid circuits rate better than wafer-scale integration.

58. This is not to say that wafer-scale logic devices are not worth developing. On the contrary, if and when wafer-scale technologies have been fine-tuned, logic and system-level WSI might find a niche for it-self. When that time comes, however, comparable advances may have been made to improve the capabilities of the competing technologies. With respect to printed board technology, it does not appear that WSI will have any serious impact within the near future. As Table 6 shows, hybrid technologies are, and will continure to be, of more concern.

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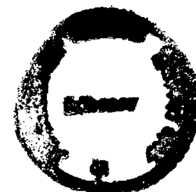


TABLE 6 ✓

Figures-of-Merit for WSI Versus Typical Packaging Technologies
(100-MHz Clock Rate)

Package	Power Versus delay (normalized)	Size or Weight (normalized)	Cost (normalized)	Overall figure-of-merit
Printed circuit board	1.00	1.00	1.00	1.00
Thick-film multilayer on ceramic	1.08	0.42	1.02	0.46
Ceramic multilayer hybrid	0.34	0.20	0.65	0.044
Thin-film multilayer hybrid on various substrates, populated on one side	0.19	0.14	0.60	0.016
Wafer-scale integration	0.01	0.09	0.46	0.0041
Thin-film multilayer hybrid on various substrates, populated on both side	0.08	0.07	0.44	0.0025

Source : General Electric Corp.

59. <u>Silicon-on-Sapphire Devices</u>. In a silicon-on-sapphire (SOS) circuit, an isolating monolithic sapphire substrate is used as the circuit carrier. A thin silicon epitaxial film is grown on the sapphire surface, and transistors are then fabricated in the film by means of conventional CMOS technology.

60. Complete isolation is achieved between each device on the chip as a result of the use of the sapphire substrate. By virtue of this di-electric isolation, SOS is inherently immune to the destructive, high-current condition known as "latch-up." (Conventional CMOS must be processed with a special epitaxial layer to prevent latch-up.) This also helps to account for its exceptional resistance to transient radiation and "single-event upset" faults, which have been known to cause faults in integrated circuit memory cells.

61. The sapphire substrate also results in very low parasitic capacitances. This, in turn, results in higher circuit speed and lower power dissipation than is possible with bulk silicon MOS devices. Other comparisons between SOS and bulk silicon are shown in Table 7.

62. Unfortunately, the use of SOS has not been price-competitive in the marketplace because of higher manufacturing costs (wafer material, photomask replacement and dicing), lower demand, and fewer companies producing sapphire wafers. This will perhaps change when more semiconductor manufacturers adopt the technical advantages of SOS.

TABLE 7

Silicon-on-Sapphire Versus Bulk Silicon CMOS

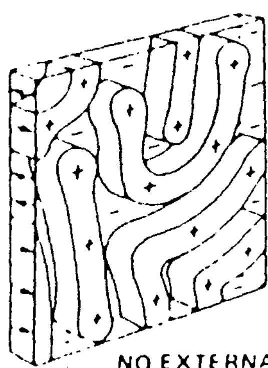
Parameter	SOS	Bulk
Design flexibility	Higher	Lower
Speed	Higher	Lower
Power dessipation	Lower	Higher
Flicker noise	Higher	Lower
Leakage Current	Higher	Lower
High-temperature performance	Better	Worse
Latch-up	No	Yes
Radiation tolerance	Higher	Lower
Packing density	Higher	Lower
Wafer material cost	Higher	Lower
Yield (4 - micro meter)	Equal	Equal
Yield (2 - micro meter)	Higher	Lower

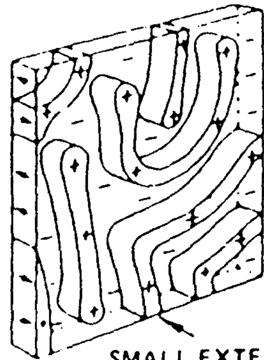
63. Fortunately, an SOS process requires fewer masking steps than a silicon-gate bulk process, which of course gives SOS a yield advantage. This advantage increases with reductions in feature size. This will probably be the determining factor in wider acceptance of CMOS/SOS circuits.

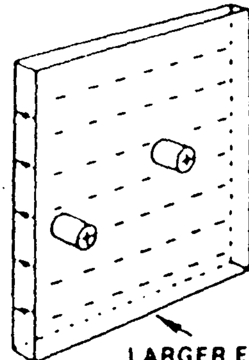
64. **Magnetic Bubble Memories**. Magnetic bubble memory devices are manufactured using techniques that are typical of the semiconductor industry at large. The heart of the device is a chip whose top surface consists of a thin film of a magnetically uniaxial material on which is deposited an array of control elements. The magnetic material has been specifically created so that its "easy" axis of magnetization is normal to the plane of the thin film.

65. In the absence of any external magnetic field, the domain structure of the thin film has an antiparallel "stripe" pattern arranged, for minimum energy, to give zero net magnetism (Fig 8). If a bias field is applied perpendicular to the plane of the film, it becomes energetically favorable for the antiparallel domains to shrink.

66. When the field is increased still further, these islands contract under pressure from the applied field to form cylindrical domains. These cylindrical domains are the "bubbles". If the field is increased still further, the bubbles will totally collapse, leaving a magnetically saturated sample. Thus, binary data is stored as the presence or absence of bubbles at addressable locations.







MAGNETIC BUBBLE MEMORY FORMATION

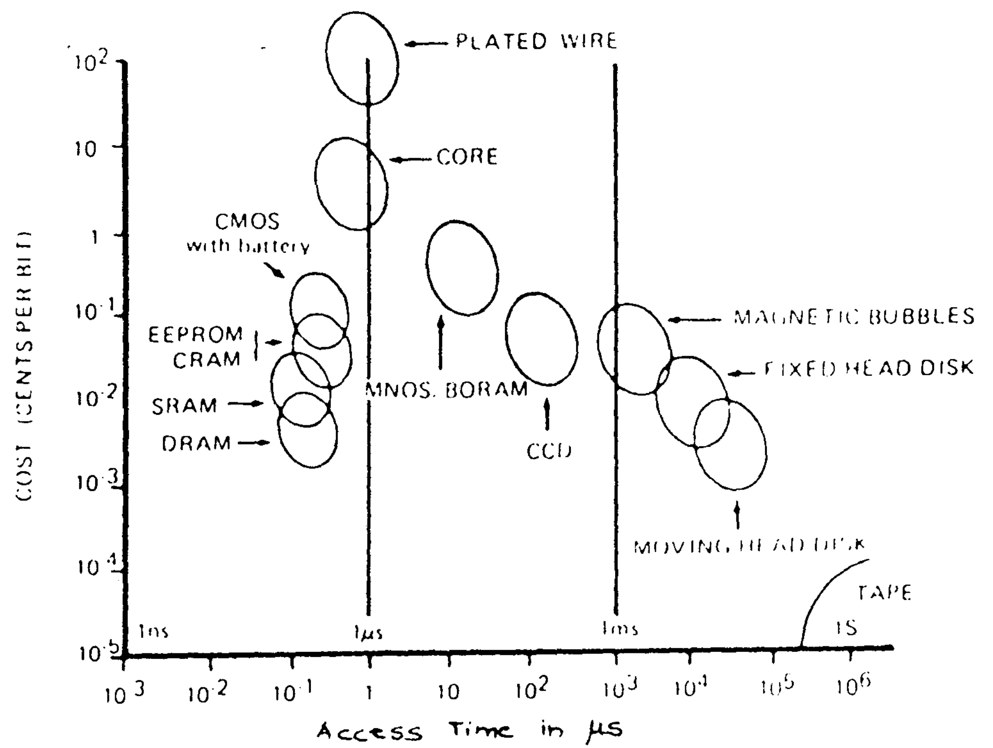
FIGURE - 8

67. As sophisticated (and complicated) as all of this may seem, magnetic bubble memories offer an attractive alternative to other media, such as tape and disk, for reliable data storage in harsh environments. Their high packing density, ruggedness, reliability, nonvolatility, and nuclear hardness also make them well suited for military applications.

68. Although not a technical issue, cost is a key consideration when selecting a memory device. For severe environment applications, for which magnetic bubble memories are best suited, ruggedized disk, and tape drives are slower but offer a lower cost per bit (Fig 9). At the other end of the spectrum, the access times of magnetic bubble memories cannot compete with random-access semiconductor memories (RAMs).

69. Therefore, if magnetic bubble memories are to find a place for themselves in the marketplace, it will have to be in applications that can accept their slower access times or higher costs per bit in exchange for improved data security, environmental stability, radiation tolerance, and potential savings in reduced maintenance costs (Un-fortunately, although several device manufacturers have entered the field, most of them have retracted as it became evident that the technology has a smaller market than was originally predicted).

70. <u>SUMMARY</u>. There appears to be no near-term letup in the increasing capability and complexity of the semiconductor technology. In fact, if anything, the pace of new developments seems to be quickening. Added to this is the general trend



MEMORY DEVICES: COST PER BIT VS ACCESS TIME

FIGURE - 9

toward having more custom and semicustom integrated circuits available to the circuit designer. These new devices offer many new capabilities to the designer, along with a more complex selection process.

71. In the past this selection process by the circuit designer was done, to a great extent, without giving major consideration to its impact on printed board technology. It was generally felt that board technology would continue to evolve to more sophistication along with advances in chip-level technology.

72. However, the new options available to the circuit designer are becoming more dependent on the cost and performance of the next-level packaging/interconnecting structure.

73. As the cost of system integration, such as printed board costs, goes up, the economics of reducing total chip count tends to push toward systems with fewer, more complex chips. There is also a general improvement in circuit performance with the use of fewer devices. Therefore, a final design decision as to which implementation of the subsystem to develop must take into account factors such as these and, hence, is not a trivial task. Therefore, the circuit designer is becoming more of a system designer, and vice versa, than he has been in the past.

SURFACE MOUNT ELECTRICAL COMPONENTS

General

74. Electronic component packages serve to protect the devices within them from the environment, provide communication links, remove heat, and provide a means for handling and testing. With larger, higher-density integrated circuits (ICs), these functions will not only continue to be important, they will be more challenging to meet. At the same time, there will be an emphasis on maintaining or decreasing the costs of the more complex packages. This will require increases in functional density and higher-performance designs as device density continues to improve dramatically.

75. Package Design Factors. There are several interrelated package design factors for advanced IC components. Some of the interrelated factors impact others very strongly. In the package design stage, one such factor may be emphasized for a given application. Examples are package electrical performance for a high-speed chip, or cost for a lower-performance device. Such trade-offs are common depending on the applicaion. Therefore, the characteristics of each package must be clearly understood in order to make the optimum selection.

(a) Cost. One must consider, in addition to the package cost itself, the sum of the cost increments of the interfacing factors of handling, testing, insertion equipment, repair procedures, inventory, multiple ...

and reliability criteria. In other words, the packaging cost factor must be viewed not only in terms of the related design trade-offs, but also in terms of the change in overall system cost.

(b) **Electrical Performance**. Another driving force in package improvement is system electrical performance. Package size reduction may go hand in hand with lower cost and higher speed due to the use of chip carriers. Also, lead lenghts are more uniform in the chip carrier designs than in the small-outline IC (SOIC) configurations. The cost savings for plastic packages can be substantial. However, for high-power, hermeticity, and maximum reliability, ceramic packages might be used.

(c) **Functional Density**. Functional density increases have occurred as IC chip complexity and lead count have increased, through reduced lead-to-lead spacing on the device package. As this trend continues, one of the consequences is higher tolerances on the package features and substrate terminal areas.

76. **Semiconductior Packages**. A very-large through-hole-mount DIP can supply the more than 40 pins that most complex IC chips demand. But since 3-in.-long components take up a lot of space, designers are turning to more exotic but more appropriate packages (Table 8).

TABLE 8

Typical Integrated Circuit Packages

LSI Package type	Maximum number of leads	Method of attachment	Removal from board	Board area including leads (in.)	Hermetic Seal
Cofirerd ceramic DIP	64	Wave solder or socket	Difficult	3.2 x 0.900	Yes
Cerdip	40	-do-	-do-	2 x 0.600	Yes
Plastic DIP	40	-do-	-do-	2 x 0.600	No
Cofired ceramic chip carrier	156 @ 0.050 in.	Socket	Simple	0.460 X 0.430 (40 lead)	No
Loaded chip carrier	156 @ 0.050 in.	Reflow solder	Simple	0.770 x 0.770 (36 leads)	Yes
Minipak	28	Reflow solder	Simple	0.500 x 0.500	Yes
Flatpack with leads out all four sides	64	Reflow solder	Simple	Approx. the same as leaded chip carrier	Yes
Ceramic substrate with clips on four sides	Upto 156	Reflow solder or socket	Simple	0.650 x 0.650 (44 lead)	Yes
Plastic premolded chip carrier	Upto 156	Reflow solder or socket	Simple	0.450 x 0.450 (44 lead)	No
Leadless inverted device (LID)	40	Reflow solder	Simple	0.450 x 0.450	No
Film carrier	40/64	Reflow solder or Wire-bond	Simple	About 0.312 x 0.312 (40 lead)	No

77. To pass on all of the high performance of large-scale integration (LSI) to the overall system, the package must be capable of holding a 0.350-in. (350 mil) square chip,, with lead counts of up to and over 80, while dissipating as much as 5 W of power. Until recently, DIPs have housed about 95% of all LSIs. However, moulded-plastic DIPs are comfortable with no more than 40 leads and only at the lower, metal oxide semiconductor (MOS) levels of power dissipation.

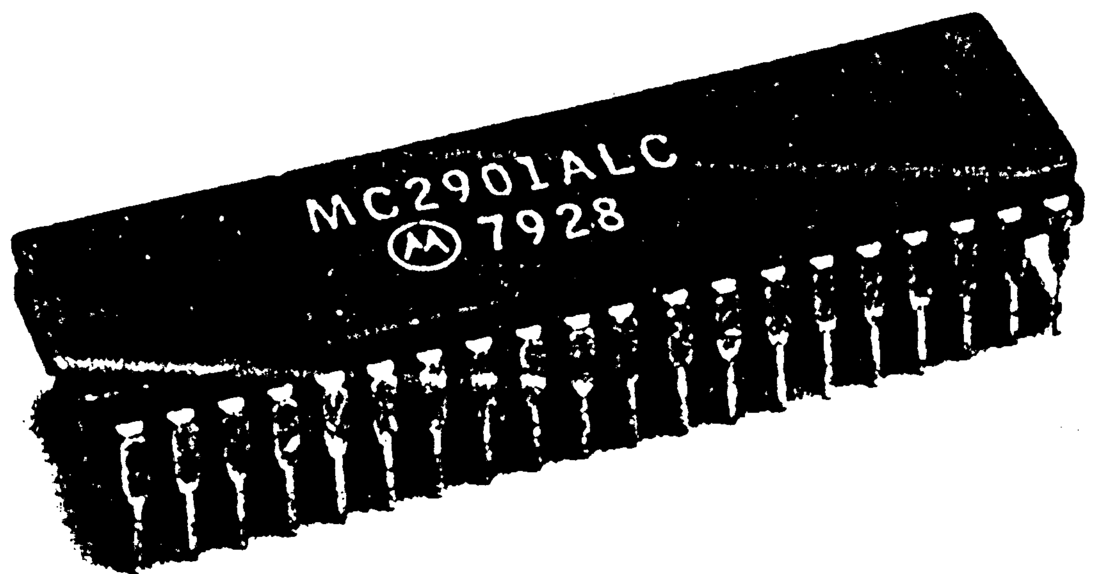
78. Cofired, heat-sunk ceramic DIPs with up to 64 leads do better. But the rival ceramic chip carrier occupies about one-third the space and also degrades chip performance less because its lead resistance is lower.

79. **Dual-Inline Packages (DIPs)**. Four significant factors have, in large part, caused the popularity of the DIP (Fig 10) :-

(a) The DIP has served both electrical and mechanical constraints of the industry well throughout its 20 years of use.

(b) Pin counts (I/Os) have ranged from 8 through 40 leads. These are the most popular pin counts, with over 75% of the devices being housed in these types with 14- and 16- lead pin configurations.

(c) Intensive capital investments have been made in all types of handling, assemble, and test equipment based on the DIP package.



FORTY LEAD DUAL - IN - LINE PACKAGE (MOTOROLA)

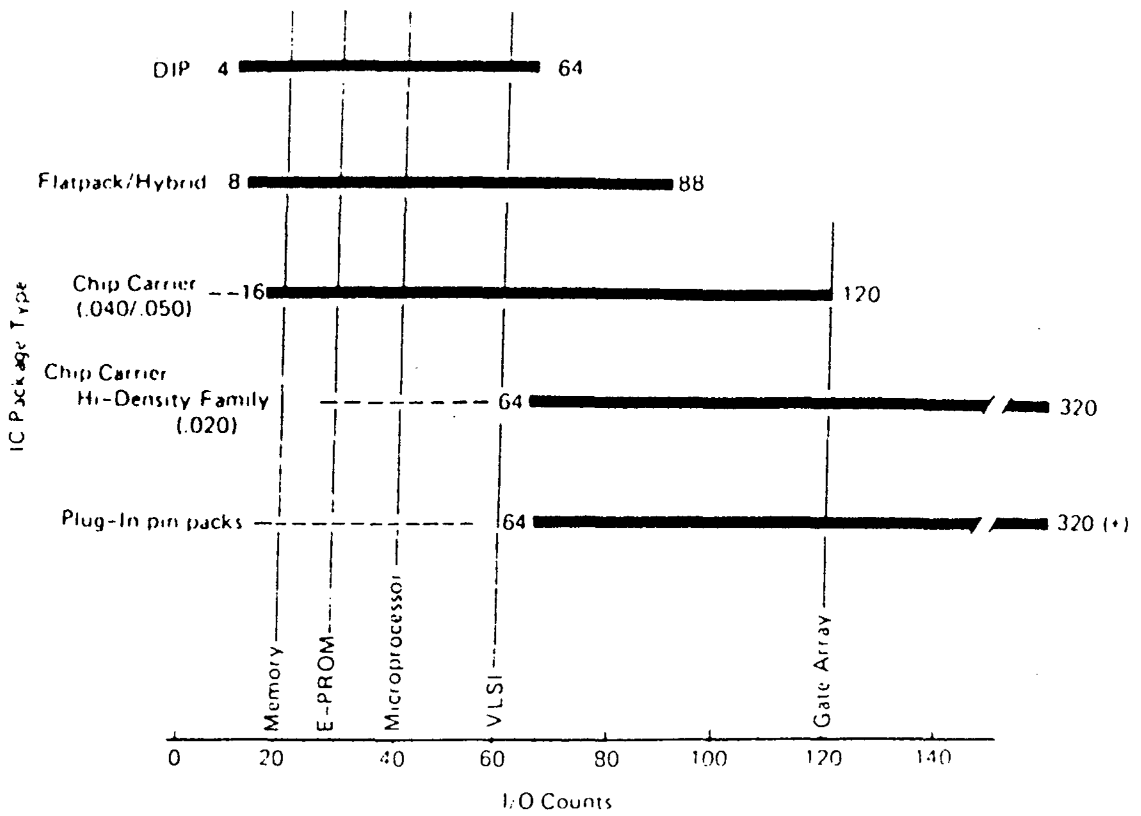
FIGURE 10

(d) DIPs are readily pluggable, with easy socketing for testing and maintenance.

80. Still, what of the future? Can DIPs remain the standard bearer and still meet tomorrow's needs? Examining the new generations of ICs, it becomes readily apparent that the DIP cannot function as well for input-output (I/O) counts above 48 (Fig 11). As semiconductor manufacturers achieve submicron feature size in chip geometries and package hundred of thousands of active devices on a chip with over 60 I/Os, the DIP will not make it.

81. <u>Chip Carriers</u>. Chip carriers can be generally described as being low-profile, rectangular (usually square) packages with I/O connections on all four sides. The I/O connections consist of metallized terminations on "leadless" versions and leads formed around or attached to the side of the package in the "leaded" versions. General selection considerations for these packages are listed in Table 9.

82. Recognizing that no one outline can satisfy all semiconductor packaging requirements, the Joint Electronic Device Engineering Council (JEDEC) has established a standard for chip carriers (CCs) that allows for multiple design approaches, manufacturing techniques, and attachment means, thus enabling designers to choose and tailor packages to their applications. The JEDEC has standardized two basic package styles (one with 0.050-in. center terminal spacing and another with 0.040-in.



I/O INTERCONNECTION RANGE FOR VARIOUS IC PACKAGE TYPES

FIGURE-11.

TABLE 9

Chip Carrier Application Considerations

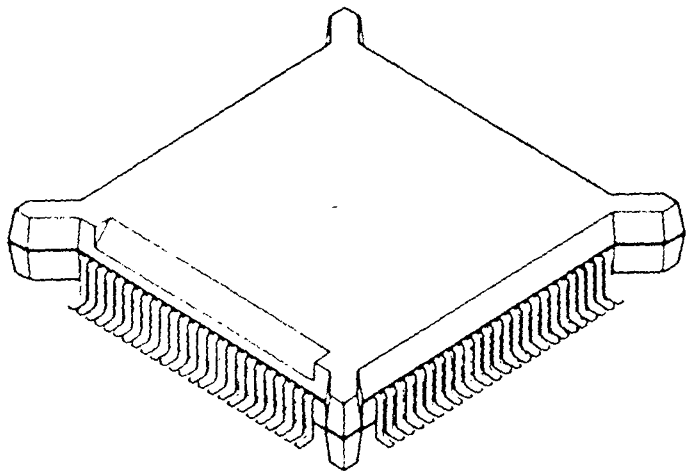
Consideration	Leadless CCs	Leaded CCs
Thermal expansion to match	Critical	Less critical
Removal and replacement	Comparatively easy with special tools	Less risk of damaging
Solder joint inspection	Difficult	Less difficult
Flux removal after soldering	Difficult	Less difficult
Socket compatible	Yes (except type C)	Yes (except type B)
lead length	Minimal	Moderate (inductance greater)
Conductive cooling	Good, with direct lead conduction path (lower profile height)	Poor (higher profile height)
Preparation for soldering	Solder coating of terminals required	None except for solder coating as required for solderability.
Self-centering	Usually	Rarely
Flexure of substrate	Critical	Less critical

spacing outlines, so that designers can interchange types to suit changing requirements without redesigning the interconnecting assembly.

83. <u>Flatpacks</u>. Flatpacks are the oldest type of integrated circuit package for surface mount applications, with their original use dating back to the early 1960s. The typical dual-row flatpack has leads on both sides of its body on 0.050-in. centers. They are supplied with from 14 to 50 flat ribbon leads. Therefore, the dual-row flatpack's leads are usually formed prior to assembly in a "gullwing" fashion for surface-mount applications.

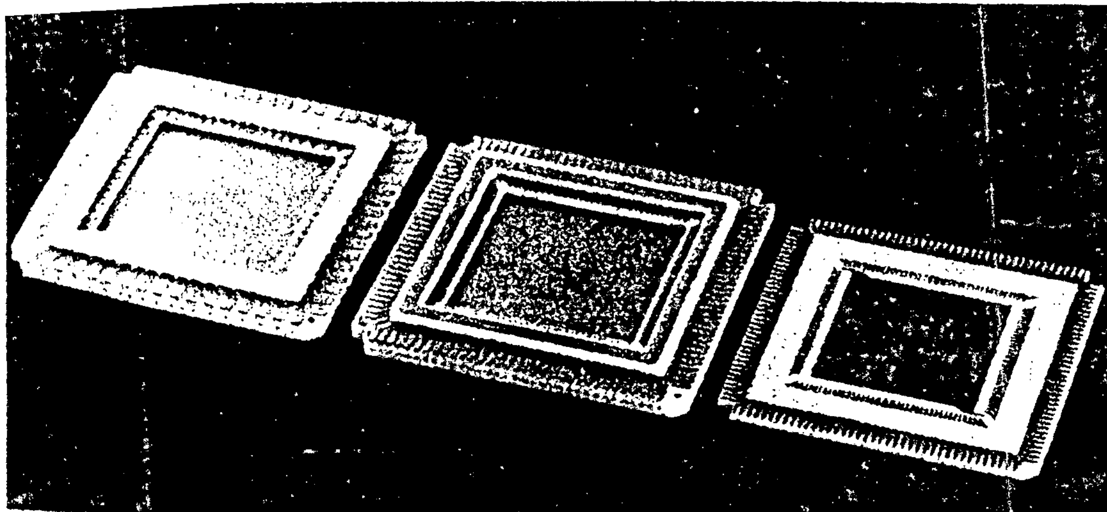
84. A new leaded integrated circuit package that is gaining in popularity is the plastic "quad" flatpack (PQFP). The PQFP (Fig 12) is a high-density/low-cost JEDEC-approved package for lead counts from 52 to 244 terminals. It utilizes a small 0.025-in. lead spacing to achieve high density and a small footprint. The PQFP also features a gullwing leadform and moulded "bumpers" in the corners to protect the leads from mechanical damages.

85. <u>Grid Arrays</u>. The higher the I/O lead count becomes, the lower the percentage of the total package area that any given size die cavity will occupy. (For example, the 96-lead, 40-mil center chip carrier is over 1 in. square.) For optimum packaging density, this percentage should be as high as possible. Therefore, for high-I/O applications, 0.025- and 0.020-in. chip carriers (Fig 13) and grid arrays are used.



PLASTIC QUAD FLATPACK (PQFP)

FIGURE - 12



LEADLESS CERAMIC CHIP CARRIERS

FIGURE -13

General Selection Criteria

86. The selection of materials for conventional (multilayer) boards and the newly emerging composite structures is important (and complicated) for thermal, mechanical, and electrical system reliability reasons. Each condidate material or combination of materials has a set of properties with particular advantages and disadvantages (Table 10). It is probable, however, that no single material will satisfy all design needs or applications. Therefore, a compromise of material properties should be sought that offers the best "tailoring" to suit end-product requiremets cost-effectively.

Organic Base P&I Structures

87. **Conventional Printed-Wiring Boards** The "king" of laminates for organic-base printed wiring boards is still the FR-4 (GF) materials. However, laminate manufacturers offer a variety of alternative materials to meet higher-performance multilayer board needs, such as polyimide (GI), multifunctional epoxies (FR-5), bismalemide-trazine (BT), and other engineered rsin systems. Driven heavily by military requirements for improved reliability, in-service thermal performance, and field repairability, the polyimides have evolved as the most significant new material in the high-performance laminate marketplace.

88. **Special Reinforcement Materials**. With the increasing emphasis on surface mount technology, new multilayer board

	Units	ASTM test method	Thermoplastics					Thermosets	
			Crystalline		Amorphous		Cryst./ amorp. blend		
			Poly-phenylene sulfide	Polyethylene-terephthalate	Poly-etherimide	Poly-ether-sulfone	Modified polyarylether	Diallyl phthalate	Phenolic
Mechanical									
Tensile strength	kpsi	D-638	17.5	22.0	24.5	18.0	15.9	9.0	9.0
Elongation at break	%	D-638	0.9%	2.3%	2.7%	3.0%	1.5%		0.2%
Flexural modulus	Mpsi	D-790	1.70	1.50	1.20	0.86	1.34	1.80	1.80
Tensile impact strength	ft-lb/in.(E2)	D-1822	9				16		
Izod impact strength, 1/8 in.	ft-lb/in.	D-256							
Notched			1.3	1.6	2.0	1.5	1.0	1.0	0.9
Unnotched			4.5		8.0	8.0	7.8		
Thermal									
Coefficient of thermal	in/in F	D-696	1.2E-5	1.1E-5	1.1E-5	1.5E-5	1.5E-5	1.5E-5	1.3E-5
Heat deflection lamp									
at 264 psi	F	D-648	500	435	410	420	293	450	500
	C		260	224	210	216	145	232	260
at 64 psi	F	D-648			414		381	450	500
	C				212		194	232	260
Limiting oxygen index	%	D-2863	46.5	33		40		50	
UL									
Thermal ind., w/impact	C	UL-764B	200	150	170	180	150	130	150
UL94 flammability		UL-94	V-O	V-O	V-O	V-O	V-O	V-O	V-O
Thickness	inches		0.028	0.032	0.063	0.017	0.032	0.058	0.067
Electrical									
Dielectric strength, 1/8 in.	V/mil	D-149	450						
Short time			363	430		375	455	400	475
Step by-step			383				419	400	425
Diel. constant, 60 Hz		D-150	3.9	3.6			3.8	4.1	5.6
1 MHz			3.8	3.6		3.5	3.7	4.0	5.2
Dissipation factor, 60 Hz		D-150	0.0006	0.0040			0.0089	0.0090	0.0290
1 MHz			0.0014	0.0100		0.0060	0.0086	0.0130	0.0250
Arc resistance	sec	D-495	38	117	85		125	130	180
Volume resistivity	Ω-cm	D-257	4.5E16	1.0E15	3.0E16	2.0E16	1.6E16	1.0E15	1.0E9
Surface resistivity	"	D-257		1.0E14			2.1E16		
General									
Specific gravity		D-1505	1.60	1.67	1.51	1.51	1.47	1.90	1.73
Mold shrinkage, MD	mil/in.	D-955	2	2	2	3	2	2.4	1.5
TD	mil/in.		10	9			5		

TYPICAL CONNECTOR BODY INSULATING MATERIALS

TABLE 10

reinforcement materials are being developed. For CTE- sensitive applications, the most interesting developments have been with respect to the use of quartz fabric and aramid fiber materials.

(a) **Quartz Fabric Materials**. Multiayer boards with improved CTE characteristics are made from a quartz fabric that has been impregnated with either epoxy or polyimide. Such boards may be processed in the same shop as a conventional multilayer board with essentially the same processes. However, because of the hardness of the fused silica, the tough carbide bits for drilling holes wear out much faster, which can present production problems. Also, quartz fabric materials are expensive, sometimes as much as several times the cost of epoxy glass. Yet it is quite possible that the positive aspects of using quartz fabric materials will outweigh the negative ones for some applications.

(b) **Aramid-Fiber Materials**. Aramid fiber (du Pont's kevlar) is a high-strength, high-modulus, low-density reinforcing material. When it is impregnated with either epoxy or polyimide resins, the resulting fabrics have enhanced mechanical and thermal properties.

89. The major concerns when using these materials in multilayer printed board applications are delamination and proper drilling-delamination, because the aramid fiber has a significantly lower CTE than the other dielectric materials in the board; and proper drilling, because of the fiber's high strength. However, in the

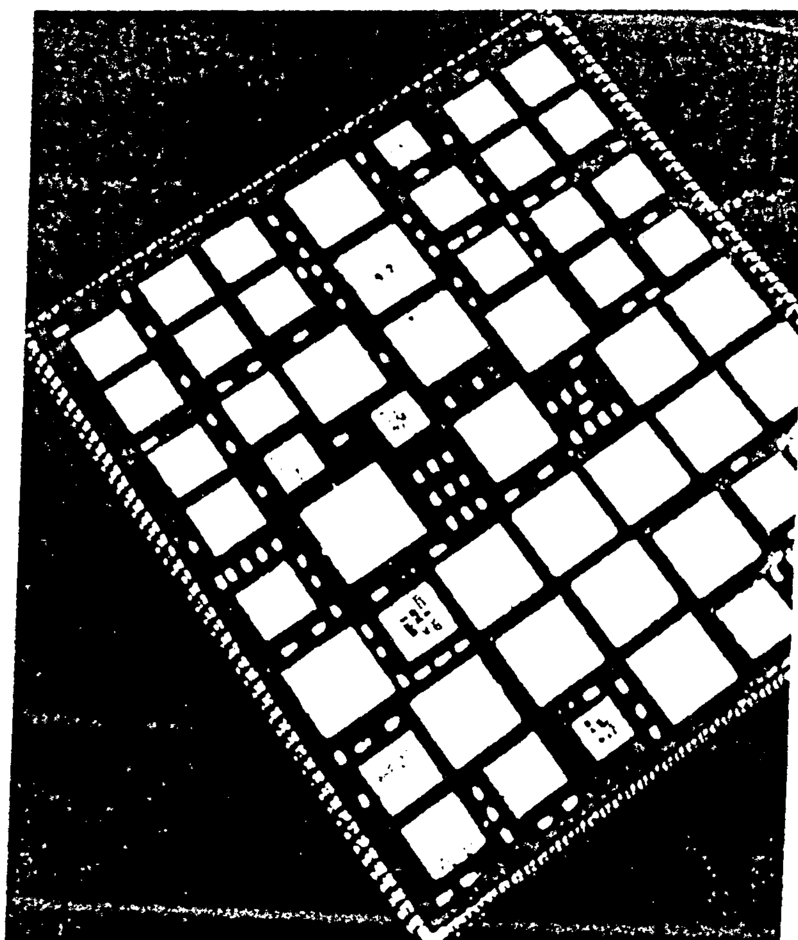
latter case there are indications that solid carbide drills can be used successfully for this purpose along with a proper set of drilling parameters and the correct entry and exit materials.

90. Copper plating of the holes in the aramid fiber laminate does not appear to present any significant problems. Procedures have been developed for electroplating these materials that have resulted in copper depositions that are virtually identical in appearance to those on conventional multilayer boards.

91. **Non Organic (Ceramic-Based) P&I Structures**. Before the development of chip carries, hybrid circuit manufacturers tended to use bare chip-and-wire techniques for IC mounting and interconnection. However, the disadvantage of this approach is that bare chips, once mounted, cannot be pretested or easily reworked. With chip carriers, which can be pretested and more easily reworked, there is no such restriction.

92. By moving to large substrates (Fig 14), the role of alumina and thick-film technology has been extended to do the tasks normally assumed by multilayer printed boards.

93. Since the whole structure is fabricated on ceramic substrates, the overall interconnection density achievable is that of 700 connections per square inch, as compared with 30 to 60 for conventianal boards. Also, conductor widths and spaces can be 10 mils; the dielectric layer can have holes or vias that can be matched to these parameters.



ALUMINA P&I STRUCTURE ASSEMBLY

FIGURE - 14

ELECTRICAL DESIGN CONSIDERATIONS

General

94. The demand for increased data processing in modern electronic systems has resulted in new high-speed digital processing technology. Thus, more capable architectures have been developed, and major advances have been made in high-speed solid-state logic devices. This is reflected in system clock speeds that are rapidly in creasing to greater than 100 MHz, and which require intergrated circuits with rise times that are frequently less than 1 nsec. Since these priorities are often in direct conflict with producibility constraints, it is important to know first how this affects the design engineer.

95. **Through-hole Versus Surface Mount Integrated Circuits**. In general, the through-hole mount dual-inline package (DIP) does not perform electrically as a comparable surface mount chip carrier as input/output (I/O) lead counts increase (Table 11). This is in part because of differences in lead and conductor lengths. The longest trace within a 64-lead chip carrier. The ratio of the longest-to-shortest DIP trace is 12.5:1, while the corresponding ratio for the chip carrier is 1.4:1. Long traces mean increased lead resistance and inductance. Unequal trace lengths affect system and device performance by restricting power and ground capabilities. Long side-to-side conductor traces result in significant lead-to-lead capacitance, which can affect some devices.

TABLE - 11

DIP AND CHIP CARRIER ELECTRICAL CHARACTERISTICS

Parameter	Lead count	Chip carrier Longest lead	Chip carrier Shortest lead	DIP Longest lead	DIP Shortest lead
Trace inductance (H)	16	1.13	0.73	6.40	1.62
	28	1.80	1.15	14.77	1.62
	40	2.90	1.87	24.94	1.62
	64	6.44	4.21	49.14	2.34
Line-to-line capacitance (pF)	16	0.13	0.09	0.74	0.25
	28	0.19	0.13	1.48	0.25
	40	0.27	0.19	2.13	0.25
	64	0.52	0.36	4.12	0.33
Trace resistance (Ω)	16	0.114	0.108	0.242	—
	24	0.139	0.136	0.319	—
	40	0.147	0.109	0.644	—
	64	0.222	0.222	1.000	—

96. One of the electronic application areas for which chip carriers offer significant advantage is that of high-speed circuitry. This rapidly growing circuit design area may well reach the point at which the packaging becomes the limiting factor in the success of the application. For instance, the circuit speeds gained with advanced semiconductors might well be lost if limiting propagation delays for 64-lead devices are 0.3 nsec for a DIP, structure delays are 0.13 nsec/in. When maximum system delay times are on the order of 0.5 to 0.3 nsec, these individual elements of propagation delay can seriously affect packaging density and power density requirements (Fig 15).

97. **Crosstalk Isolation**. Signals at high frequencies on closely spaced conductors (and the subsequent electromagnetic signal phenomena) give rise to problems associated with isolating signal lines from inductive and capacitive coupling. This induction of unwanted signals into other conductor lines from active signal lines is called "crosstalk." There are five parameters that affect the degree of crosstalk :-

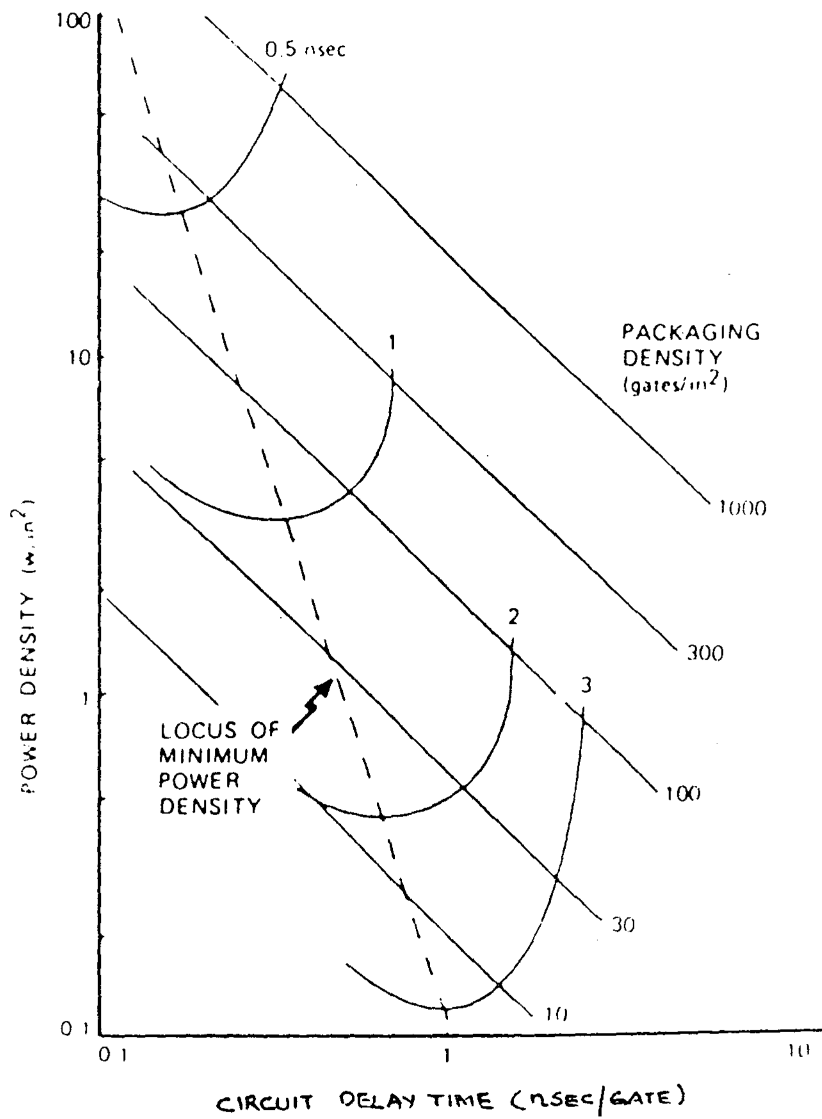
(a) The distance between conductors (the farther apart, the better.

(b) The dielectric medium (the higher the dielectric constant, the better).

(c) The presence of ground shields (the more, the better).

(d) The signal rise time (the slower, the better).

(e) The length of the coupled lines (the shorter, the better).



FACTORS AFFECTING SYSTEM DELAY TIME

FIGURE-15

98. Unfortunately, the action taken to reduce crosstalk is often in conflict with the implementation of high-density interconnections, maintaining high propagation velocities, and controlling impedance. For example, the lower the dielectric constant, the higher is the signal propagation speed; the higher the dielectric constant, the better is the electromagnetic isolation.

99. The presence of ground shields enhaces the degree of signal isolation and permits closer control of impedance values. However, the use of extra ground shields and ground planes complicates the fabrication of the printed board.

100. Another approach to reducing interlayer coupling is to route signal lines orthogonally to each other between adjacent signal layers. Intralayer reductions can be achieved by using interdigitated guard lines between signal lines on the same layer of the printed board. However, both these approaches increase conductor routing pattern complexity accompanied by requirements for higher resolution and better alignment accuracies between layers of the printed board. This, in turn, tends to reduce manufacturability and increases costs.

101. <u>Power Distribution.</u> Within the world of modern digital circuitry, most discussions have centered primarily on the theme of transmission line theory. Although not discussed as openly, the requirements for increasing power distribution bear equal consideration by the system designer. On the surface, the treatment of these two dominant concerns, speed and power, may appear to be distinct issues that must be accommodated

separately. They are, however, closely intertwined physical relationships. More specifically, although select facets of design that accommodated one aspect of power may be totally independent of speed, there are others that negatively impact it. The converse relationship is, of course, also true.

102. The power and ground planes of the more damanding circuit logic families, such as ECL and GaAs, usually must be designed using heavy copper (2 oz and grater) to provide the general electrical characteristics of increased ampacity, reduced resistance, and depreciated component (inductive and capacitive) parasitics. More specifically, the heavy ground planes are used for :-

(a) <u>Noise immunity</u>. A homogeneous/noninterrupted path improves laminar electron flow and , consequently, reduces signal transmission noise.

(b) <u>Energy Dissipation</u>. Some of the high-speed logic families consume power at an extremely high rate. This energy must, of course, be dissipated without adversely affecting the operating environment limits.

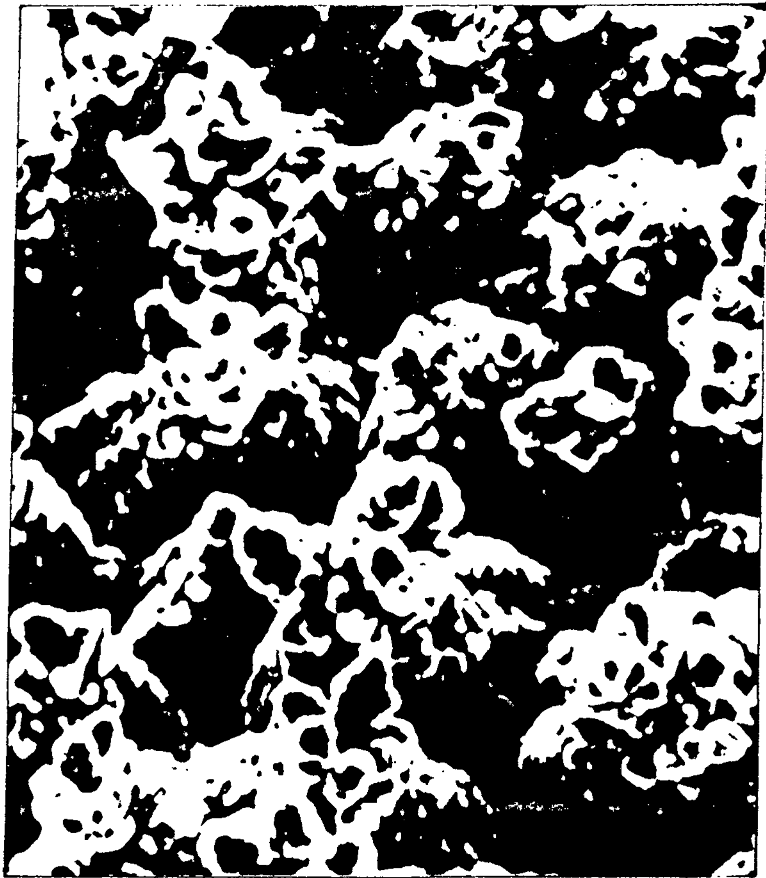
(c) <u>Current Surges</u>. Because of the switching speed and possibilities of spontaneity of switching states, excessive current surges are likely. These surges must be restrained in the system by inductive (parasitic) elimination and restraint of impendance flow.

(d) <u>State Level</u>. Owing to the reduce switching state levels and bias voltages, the system is extremely sensitive to voltage/ground level variations.

103. In addition to complicating the fabrication of printed boards, the use of heavy copper planes brings concerns as to which type of coper foil should be used, because of the phenomenon of "skin effect." The skin-effect depth is defined as that distance from the surface at which 80% of conduction occurs. This depth varies with frequency (about 2 _m for ECL circuit speeds and 1 _m or less for GaAs circuit speeds), so the conductive path mostly follows the contour of the foil.

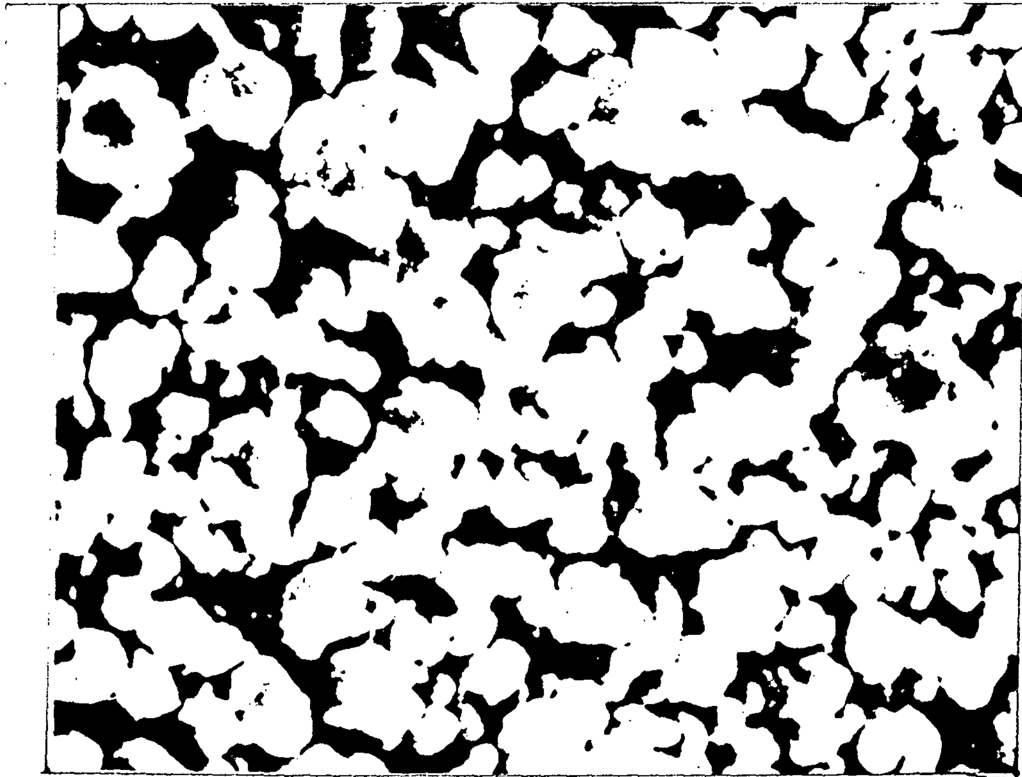
104. As a result of its fabrication process, electrodeposited (ED) foil has both a smooth and a matte side. It is supplied with a treatment on the matte side to enhance bonding of the surface to the laminate. The treatment essentially provides an additional roughness texture consisting of minute projections of copper and copper oxide that are deposited most heavily on the peaks of the tooth (Fig 16). Over these projections is deposited a second metallic layer of brass to provide stainproofing.

105. Unlike ED copper, foil made by rolling copper ingot to progressively smaller thicknesses has uniformly smooth surfaces on both sides. It too must have a surface treatment to enhance its bonding to a laminate. For this purpose, very small metallic nodules are uniformly deposited to mechanically lock the resin to the otherwise smooth foil surface (Fig 17). The treatment



ELECTRODEPOSITED COPPER FOIL

FIGURE - 16



WROUGHT COPPER FOIL

FIGURE - 17

further provides the wrought copper with a surface-stabilizing agent the inhibits oxidation and tarnish.

106. Since the conductive path basically follows the irregular contours of the treated foil surface, wrought copper foil does not display the same large increase in conductor resistance at high frequencies as does ED copper. Thus, it is better suited for these applications.

107. **Planar Resistor Technology**. It is especially effective for some computer circuit designs, such as those using emitter-coupled logic (ECL), to incorporate a large number of terminating resistors into the assembly. The use of planar resistors has proven to be a viable alternative to discrete resistors and resistor networks for several of these applications.

108. Planar resistor technology is a thin-film system that utilizes conventional subtractive printed-board fabrication methods. The laminate system consists of an insulating substrate and, rather than a single conductive layer, has a two-layer bifunctional cladding. The lower layer, immediately against the base laminate surface, is an electrically resistive material. The upper layer is copper. The two layers of this bifunctional cladding are in contact with each other over their entire area. By means of selective etching, the two layers can be etched differently so that separate conductors and resistors are formed.

109. The advantage of using this type of resistive system include :-

(a) Increased circuit density (fewer discreate components)

(b) Improved reliability (fewer solder joints)

(c) Improved electrical properties (the resistors are closer to the integrated circuits)

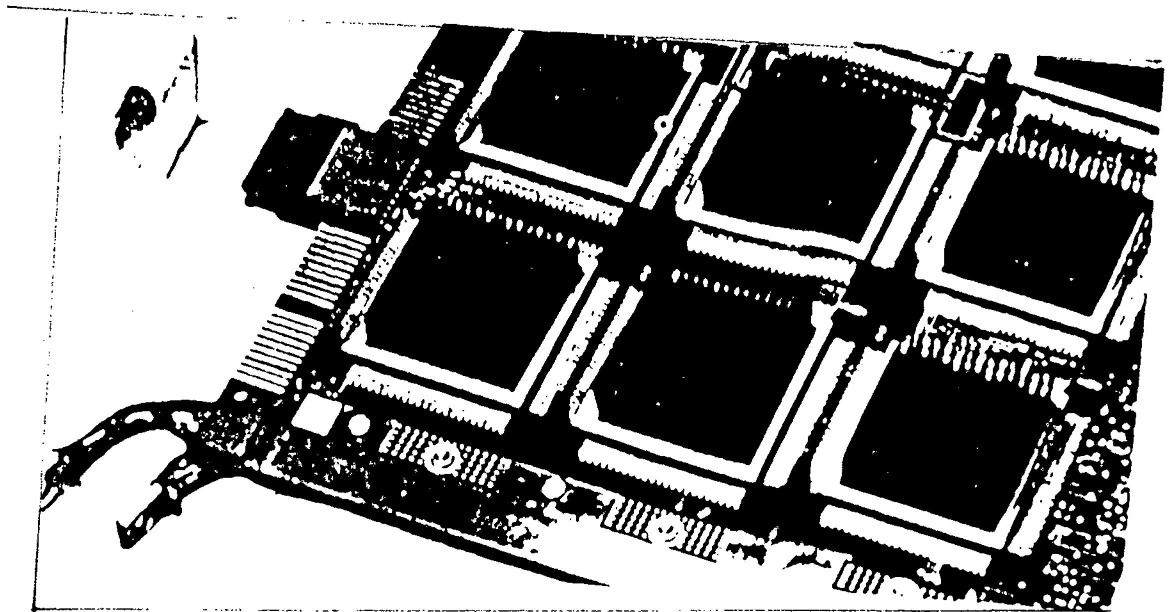
Therefore, the use of this type of resistive system depends to a great degree on the number of resistors being implemented (and the cost savings this provides) and the level of sophistication of the end-product application.

THERMAL MANAGEMENT

General

110. While the power consumed per integrated circuit (IC) function is decreasing, the number of functions per chip is increasing. This has led to increased power consumption per device. Opinion is divided on what power the VLSI the 90s will dissipate, but a norm of a few watts per device package is probable. The greatest impact on thermal management will result from having such devices mounted very close together. This means that with one 68-pin chip carrier per square inch, the power density will be on the order of a few watts per square inch.

111. Thermal Management. If the junction temperatures of the IC devices are to be held to a reasonable level, about 100 degree C, by using convection cooling or forced-air cooling in the worst case, it will certainly be necessary to have a good thermal path from the chip to the P&I structure or to its own heat sink. The



CHIP CARRIER WITH INDIVIDUAL HEAT SINK

FIGURE- 18

latter will necessitate having the heat sink as an integral part of an individual chip carrier (Fig 18) and/or having chip carriers with integral heat sinks mounted together on a mother carrier.

112. The heat concentrations encountered in today's "cutting-edge technology," as exemplified by multichip modules pose a significant challenge to the packaging engineer with respect to thermal management. Table 12 reveals that at the bare chip level within the package, these heat fluxes are in the range of 5 to 40 W/cm^2 (31 to $250W/in.^2$). The upper end of these heat densities is comparable to the thermal loading experienced by space reentry vehicles, and at the lower end to heat fluxes imposed on rocket motor cases. 117. These thermal management requirements and the critical need to reduce off-chip time delays, as well as the need to provide significantly higher system mean-time-between-failures (MTBF) values at substantially lower costs, have focused efforts on the use of multichip modules. Thus, the thermal management associated with multichip modules is, by necessity, at the forefront of thermal control technology.

113. Many sophisticated thermal management schemes exist: some are based on the cooling of the P&I structure instead of cooling the chip carriers directly, others are based on the use of forced-air cooling, and still others utilize a high degree of conduction cooling. However, no matter what the ultimate scheme chosen is, all such designs require thermal management that takes

TABLE - 12

SINGLE CHIP AND MULTICHIP MODULE THERMAL PARAMETERS

Technology	Chip size (mm)	Maximum power dissipation (W)	Maximum chip flux (W/cm²)	Thermal resistance (K/W)
Single-chip modules				
Mitsubishi Alumina HTCP	8 × 8	4	6.25	5.2
Mitsubishi SiC	8 × 8	4	6.25	4.7
Hewlett-Packard Finstrate	6.3 × 6.3	4	10.10	<8.7
Hitachi S-810	1.9 × 4	1	13.1	7.0
Fujitsu M-380	4.5 × 4.5	3	14.8	8.0
Fujitsu M-780 air-cooled	9.3 × 9.3	6.5	7.5	3.5
Fujitsu M-780 water-cooled	9.3 × 9.3	9.5	11.0	2.5
Burroughs PGA	4.5 × 4.5	5	24.3	12
Motorola MCA-2	7 × 7	12	24.5	3.3
Sperry Compact HX	5 × 5	10	40	4.9
Multichip modules				
Mitsubishi HTCM	8 × 8	4	6.25	7.3
NEC SX liquid-cooled module	8 × 8	>5.4	>8.4	5 (water-cooled)
Hitachi RAM	1.9 × 4	1	13.1	34.7
IBM 4381	4.6 × 4.6	3.8	17.0	17.0
IBM 3090 TCM	4.85 × 4.85	7	29.8	8.7 (water-cooled)
NTT grooved substrate	8 × 8	15.1	23.6	3.3 (water-cooled)

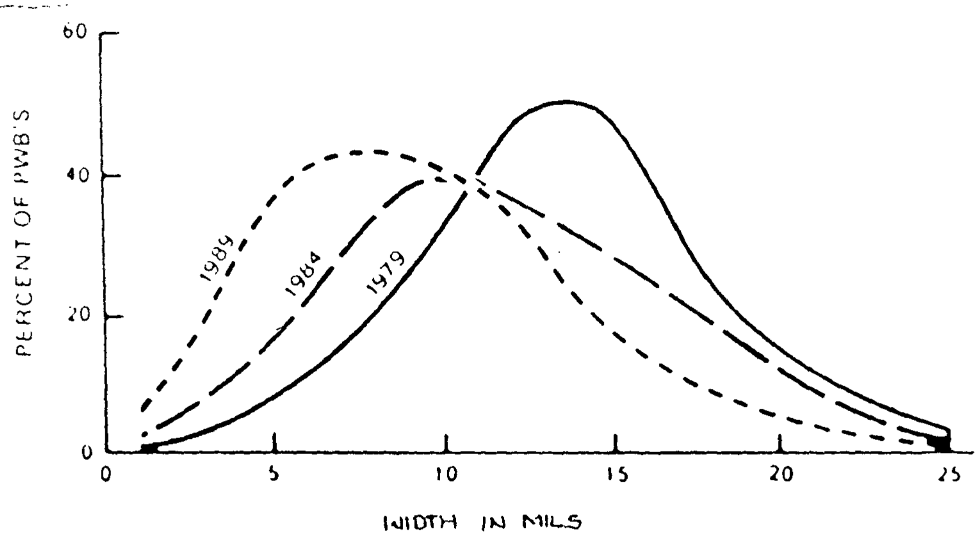
into account the thermal properties of both the chip carrier and the P&I structure. Therefore, careful consideration must be given to these elements of the packaging system when a high degree of heat dissipation is required.

PRINTED-BOARD DESIGN CONSIDERATIONS

General

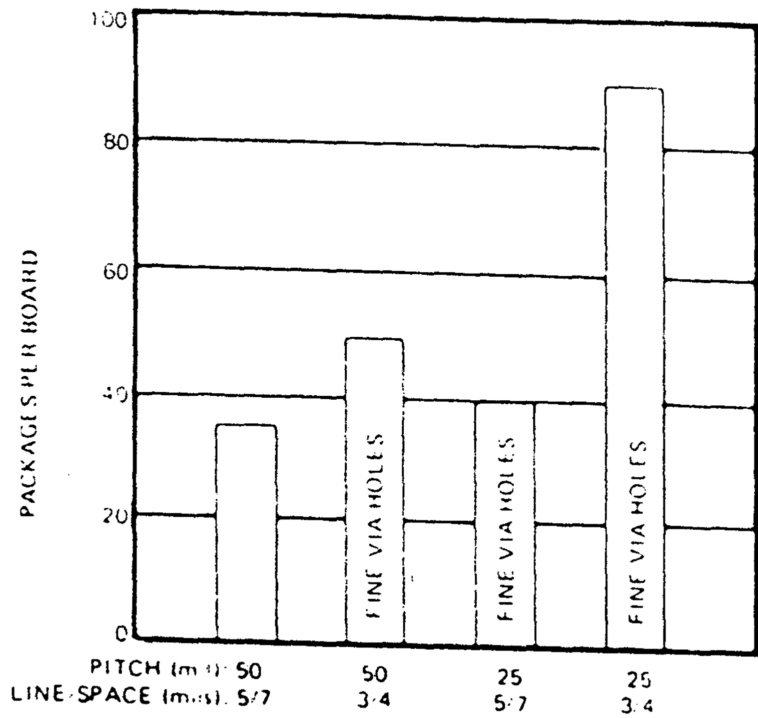
114. The continuing trend towards finer board lines and spaces (Fig 19) and the availability of thinner copper foils, preferably 1/2 oz, seem to be sufficient for current requirements for surface-mounting chip carriers. For example, approximately thirty five 84-pin chip carriers can be interconnected with two signal layers on an 8-in. x 13-in. board with a conventional 0.034-in.-diameter vias, 0.005-in. conductor widths, and 0.007-in. spacing between conductors (Fig 20). However, as the technology continues to mature, higher component densities will be required, and these land pattern features will not be sufficient. The board designer will then be forced to push for fine via holes with land diameters of about 0.020-in. along with finer line widths and spaces. As shown in Fig 20, this will provide density improvements on the order of 35% using 0.050-in.-pitch chip carriers.

115. **Board Size/Quantity**. The envisioned improvements in land pattern feature size will have a significant effect on the board area/number of layers required to interconnect a given circuit function. However, this does not mean that boards will get



PRINTED WIRING CONDUCTOR WIDTH AND SPACING TRENDS

FIGURE - 19



PRINTED WIRING DESIGN TRADE OFFS.

FIGURE - 20

smaller and the number of layers will decrease. The driving force will continue to be to put more and more circuit functions on a board. Therefore, board fabrication, assembly, and testing capabilities/limitations will probably keep board size and the number of layers where they are today.

116. Space Effectiveness. The space effectiveness (die size/package size) of a DIP is inversely proportional to the number of pins it has. For example, an 18-pin DIP requires about 0.28 in.^{2} to support a die of 0.039 in.^{2}, or is 14 % efficient as a package. In a 40-pin DIP, the die size increases to 0.05 in.^{2} with a 1.25-in.^{2} package and the efficiency drops to only 4%. In comparison, an 18-pin rectangular chip carrier requires about 0.1-in.^{2} to support a maximum die area of 0.03 in.^{2}, for a space efficiency of 30%-that is, over twice the value for an 18-pin DIP.

117. As the I/O goes to 40 pins, a leadless chip carrier that uses 0.48 in.^{2} will accept a die that is 0.25 in.^{2}, giving a slightly reduced efficiency of 26%. Thus, leadless carriers retain a relatively high space efficiency as pin count increases, while being more space-effective overall.

118. Comparison of the space required for the various chip carriers shows that for the relatively lower pin counts the fine-pitch chip carriers require less space. However, as the pin counts increase, the advantages of using the fine-pitch chip carriers decreases, especially when compared to the use of pin-grid arrays.

119. <u>Land Patterns</u>. None of the advantages of using chip carriers and surface mounting would have any real significance without the ability to properly interconnect the devices. Fortunately, the uses of chip carriers and surface mounting allows for the use of small hole sizes, dictated only by the substrate thickness and/or the through-hole technology being used. Thus, land patterns ("footprints") can be arranged to produce configurations with a routing capability commensurate with the increased packaging density.

120. A common land pattern design guideline for both reflow-soldered and wave-soldered assemblies for resistors is

Land width (X) = $W_{max} - K$

Land length (Y) = $H_{max} + 2T_{max} + K$

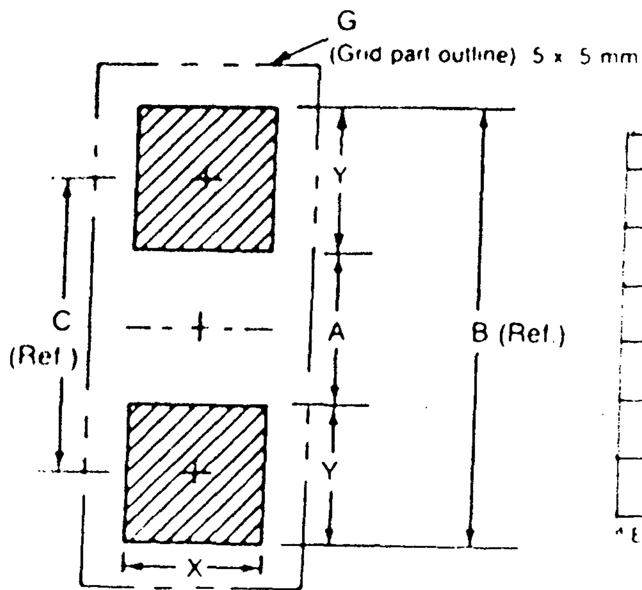
Gap between lands (A) = $L_{max} - 2T_{max} - K$

where

W = component body width
H = component body height
L = component body length
T = solderable termination thickness
K = constant of 0.25 mm (0.010 in.)

121. When all the numbers derived from this equation are rounded to the nearest sensible land size, taking into account that board processing tolerances can reduce or enlarge the conductive pattern, land patterns for resistors can be developed like those shown in Fig 21.

122. For capacitors, the equation is modified slightly due to the height of the metallization. For most capacitors, except tantalum, the land length formula becomes

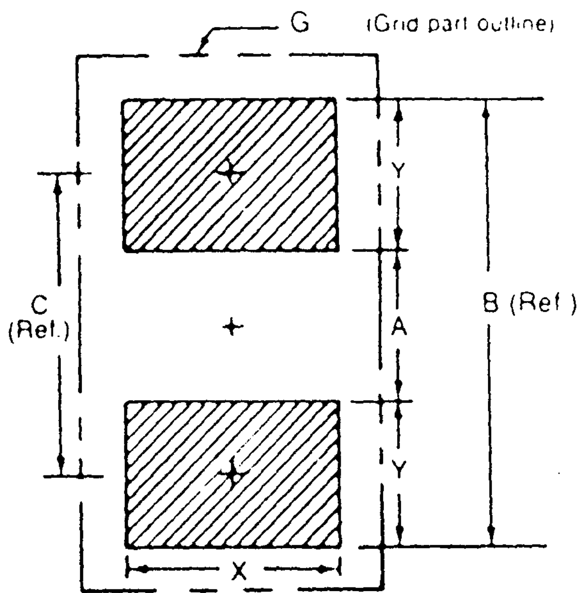


Code Letter	RC 0805	RC 1206*	RC 1210
A	0.8 [.032]	1.8 [.070]	1.8 [.070]
B	3.8 [.150]	5.0 [.200]	5.0 [.200]
C	2.3 [.090]	3.4 [.134]	3.4 [.134]
X	1.4 [.055]	1.6 [.063]	2.6 [.102]
Y	1.5 [.060]	1.6 [.063]	1.6 [.063]
Grid part outline	4 x 8	4 x 12	6 x 12

* Example shown in graphics

LAND PATTERN FOR RECTANGULAR CHIP RESISTORS

FIGURE - 21



Code Letter	CC 0805	CC 1206	CC 1210*	CC 1812	CC 1825
A	0 8 [032]	1 8 [070]	1 8 [070]	3 2 [126]	3 2 [126]
B	3 8 [150]	5 0 [200]	5 4 [213]	6 8 [268]	6 8 [268]
C	2 3 [090]	3 4 [134]	3 6 [142]	5 0 [200]	5 0 [200]
X	1 4 [055]	1 6 [063]	2 6 [102]	3 2 [126]	6 6 [260]
Y	1 5 [060]	1 6 [063]	1 8 [070]	1 8 [070]	1 8 [070]
Grid part outline	4 x 8	4 x 12	6 x 12	8 x 16	14 x 16

* Example shown in graphics

LAND PATTERN FOR RECTANGULAR CHIP CAPACITORS

FIGURE - 22

Land length (Y) = $H_{max} + T_{min} - K$

Determining land width and gap is the same as for resistors. Typical land patterns for capacitors are shown in Fig 22.

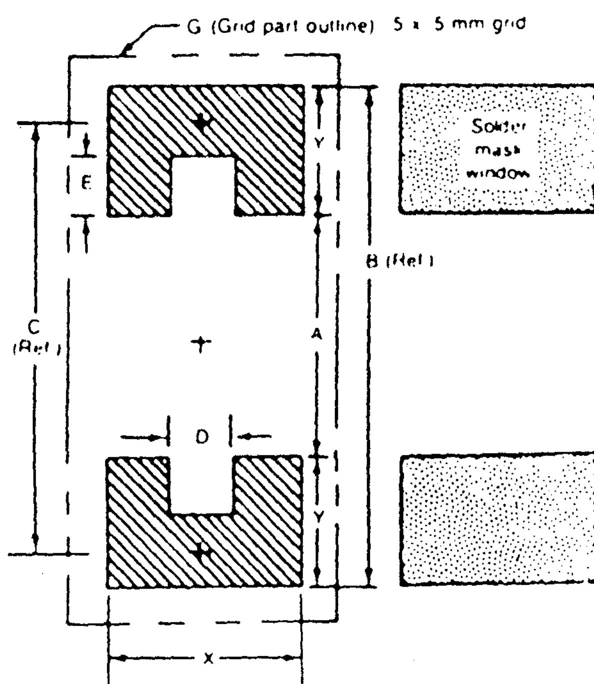
123. When tublar metal-electrode-face (MELF) components are used, cutouts in the rectangular areas of the land pattern (Fig 23) have been found to be helpful in holding the component in place during an automatic reflow soldering process. They may be omitted if other processes are used.

Spacing

124. **Component Spacing**. The land pattern design guidelines discussed so far are important for the reliability of surface mount assemblies. However, the designer should not lose sight of manufacturability, testability, and repairability considerations.

125. A minimum spacing between components is required to satisfy all of these requirements. However, there is no limit on maximum component spacing; the larger, the better. Unfortunately, some designs necessitate having the components positioned as close as possible. This is not generally a good practice. Based on experience, the minimum component spacing shown in Fig 24 should be maintained for good producibility.

126. **Land Spacing**. The spacing between lands (terminal areas) for plated-through holes will vary depending on design/manufacturing requirements and, to some extent, on the method of artwork generation, i.e., manual versus photoplotter generation.



Code Letter	MELF 1/4 W	MLL34	SOD80	MLL41[a]
A	4.4 [.174]	2.2 [.087]	2.2 [.087]	3.4 [.134]
B	8.4 [.330]	5.0 [.200]	5.4 [.213]	7.0 [.276]
C	6.4 [.252]	3.6 [.142]	3.8 [.150]	5.2 [.205]
D[b]	0.3 [.012]	0.3 [.012]	0.3 [.012]	0.3 [.012]
E[b]	0.8 [.032]	0.7 [.028]	0.8 [.032]	1.0 [.040]
X	2.5 [.100]	2.0 [.080]	2.0 [.080]	2.8 [.110]
Y	2.0 [.080]	1.4 [.055]	1.6 [.063]	1.8 [.070]
G	6 x 18	6 x 12	6 x 12	6 x 16

[a] Example shown in graphics

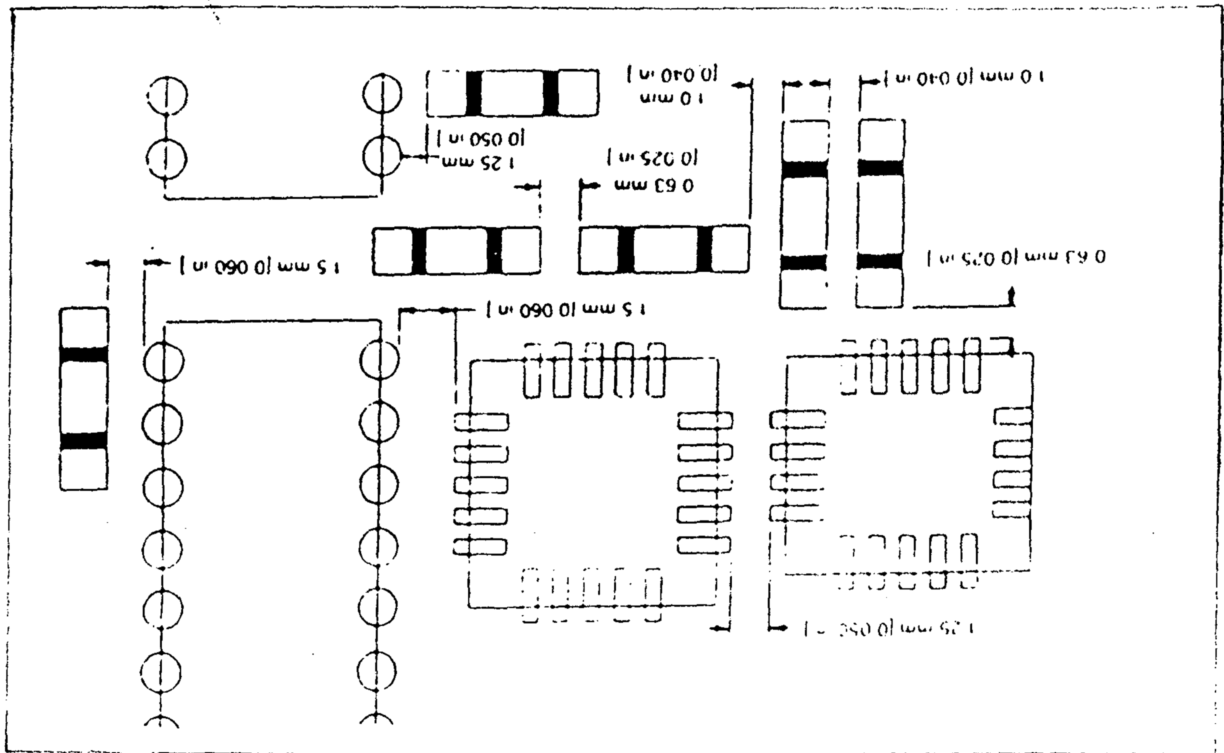
[b] The notch shown by dimensions "D" and "E" are intended to reduce skewing and are optional. The depth of this notch may be determined by the following:

$$E = Y - \left(\frac{B - L_{MAX}}{2}\right)$$

Where L equals the maximum body length

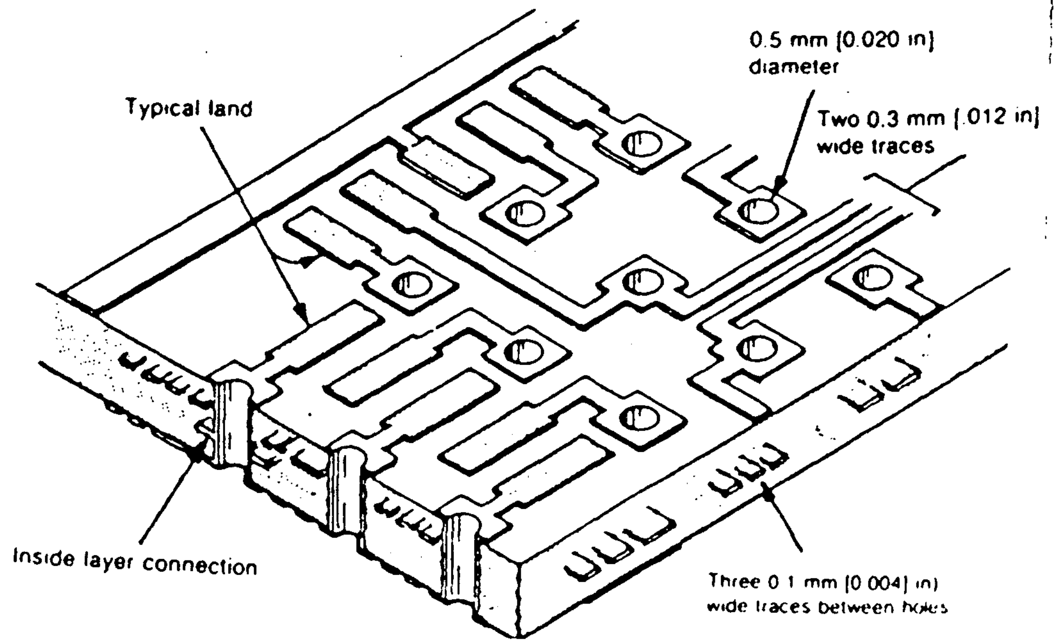
LAND PATTERN FOR TUBULAR COMPONENTS

FIGURE - 23



RECOMMENDED MINIMUM LAND-TO-LAND SPACING

FIGURE-24



LAND PATTERN TO VIA RELATIONSHIP FOR 2.54-mm GRID

FIGURE - 25

Fig 25 shows various configurations of lands for optimum conductor routing and testability..

MULTILAYER BOARD FABRICATION AND GENERAL ASSEMBLY CONSIDERATION

General

127. Many new developments are taking place in multilayer printed-wiring boards. These activities are in response to the increased demands for surface mount products that cost-effectively provide high-density interconnections that are accurately predictable and controlled within spacific value "windows." As in all rapidly advancing technologies, certain key elements provide the impetus for this progress. For example, high-density conductor patterns and high-aspect-ratio plated-through holes are becoming more readily achievable with advancements and refinements in drilling, imaging, etching, and plating technology. Thus, the new multilayer boards are becoming more than just a passive means for obtaining interconnections. Except for integrated circuits, they are becoming the most important "component" of critical high-performance electronic assemblies.

General Considerations

128. Despite their advantages, multilayer boards are not simple to make. In fact, fabricating them is a good example of the difficulties that arise when the need to shrink dimensions runs up against physical processing constraints, especially when yields, and ultimately costs, are involved.

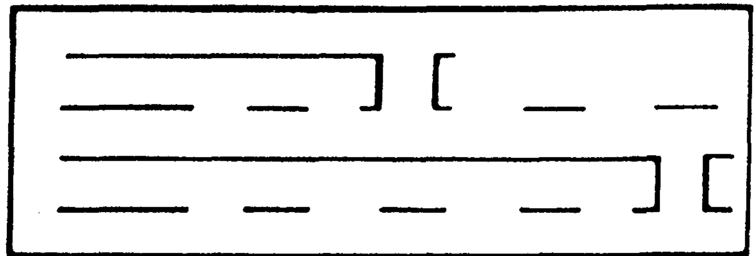
129. The suscess of a multilayer board design depends as much on the expertise of the board manufacturer as it does on the care taken by the designer. Therefore, there is a continual effort to improve multilayer board manufacturing processes in order both to increase circuit density and reduce end-product costs. The following describes a few recent developments in multilayer board processing that help achieve these goals.

Buried Vias

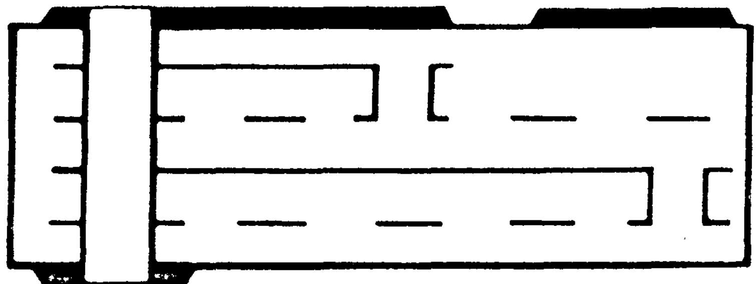
130. The use of multilayer boards with "buried" vias is one of the approaches currently being explored in order to provide higher current densities. The main advantage of buried vias construction (Fig 26) is that it allows connections to be made between internal board layers without connections to external layers. (When the connecting via goes between an internal layer and only one of the outside layers, the via is referred to as a "blind" via.)

131. Buried via multilayer board fabrication uses the same equipment, materials, and processes required to fabricate conventional boards. The major significant difference is that inner layers are made in pairs connected by small plated-through holes, which subsequently become encapsulated within the board during the multilayer lamination process. Subsequent board processing is the same as with conventional multilayer boards.

(a)



(b)



(c)

MULTILAYER BOARD BURIED VIA FABRICATION

FIGURE-26

Drilling Small Holes

132. The trend toward increased packaging density has resulted in a shifting of commonly used hold drilling• diameters downward toward 0.020 in. and less, with corresponding increases in board thickness-to-hole diameter aspect ratios. This creates several problems for the multilayer board fabricator, including :-

(a) Increased breakage of drill bits, with increased scrap rates.

(b) Lower productivity, due to the use of slower "hit" rates and lower stack heights.

(c) Higher per-hole drilling costs.

In addition, through-hole plating problems are significantly increased.

Laser Drilling

133. In order to overcome many of the problems mentioned above, small-hole drilling may require the use of special machines and processes. One such approach being explored is laser drilling, which appears to be feasible for drilling "blind" through holes in printed boards as small as 0.004 in. in diameter and less.

134. The use of lasers is receiving much attention for "blind" via-hole drilling. For these applications the use of a CO_2 laser seems to be a good choice, as both epoxy and glass are strong absorbers of radiation at the laser's wavelength, and the high

reflectivity of the copper minimizes the coupling of the laser energy into the buried land.

Component Considerations

135. In addition to providing high-density interconnections, multilayer boards are being developed that also provide capacitance, inductance, and resistance features that replace discrete circuit components. Similar rectangular circuit patterns on adjacent layers of a multilayer board separated by the board's dielectric material form "capacitors". "Inductors" can be simulated by the routing of circuitous conductor patterns.

136. Planar resistors can be formed on internal layers of a multilayer board using a laminate system composed of an insulating substrate and, rather than a single conductive layer, a two-layer bifunctional cladding. The lower layer, immediately against the base laminate surface, is an electrically resistive thin-film material. The upper layer is copper.

137. The two layers of this bifunctional cladding are in contact with each other over the entire surface area. By means of selective etching, the two layers can be etched differentially, so that separate patterns of conductors and resistors are formed.

General Assembly Considerations

138. Surface-mounted assemblies typically have many solder joints. The solder joints are identical in appearance and spacing. The repetitious nature of making and inspecting such a

large number of geometrically identical joints reduces inspection effeciency, so unacceptable joints are likely to be overlooked, even with multiple inspections.

139. Also, defects that are found are often difficult to repair, and repair procedures have the potential of introducing additional problems. In view of this, the most cost-effective assembly procedures are those that assure acceptable quality levels through samplelot inspection. Therefore, acceptable quality must be guaranteed by the proper specification of components and materials and by the use of easily controlled manufacturing processes.

140. The specifications of interest include tolerances, placment accuracy, solder mask, and solderability.

(a) <u>The Dimensional Tolerances of Both The Chip Carrier and the Packaging and Interconnecting (P&I) Structure</u>. For high soldering yields with 50-mil-center chip carriers, a 0.002-in. Planarity and a 0.005-in. lateral lead location tolerance is required. Also, surface mounting often requires a 0.5% or better warpage limit.

(b) <u>The Accuracy of Device Placement</u>. Studies have shown that leaded chip carriers must be placed within 0.005-in. of their true position. This value can be somewhat higher for leadless devices, due to the self-centering nature of the soldering mechanisums involved.

(c) The Registration of the Solder Mask. To permit acceptable solder fillet formation, the registration of the solder mask must be located within 0.005-in. or better of its true position.

(d) The Solderability of the Materials to be Joined. Solderability specifications for both the chip carrier and the P&I structure should permit acceptable wetting of all joint surfaces, even after inventory storage of the components.

141. Solderability testing of components is not a new requirement. However, its value to the use of chip carriers and surface mounting is much more pronounced. Since the final solder joint is not always completely visible, it is almost impossible to ensure visually that each terminator has been properly soldered. Therefore, considerable attention must be given to ensuring solderability before components are installed on assemblies. This will probably lead to increased use of automatic solderability testers because such equipment becomes more available and when its use can justified for inspecting components at higher sampling rates than are presently used.

142. **Solder Deposition**. Solder must be supplied to the joint sites in a sufficient quantity to close all gaps between the chip carrier leads and the termination land that results from nonplanarity of the leads and/or substrate warpage. In addition, when soldering to gold-plated leads, solder of sufficient volume

possibility of joint failure due to gold embrittlement. Several methods are potentially available to supply the required amount and location of solder. However, only those with a high degree of control are suitable.

143. **Electroplating**. Electroplating is not as well suited as solder depositions, as might first be thought, because of difficulties encountered in controlling alloy thickness where nonuniform geometries exist; long plating times required for thick depositions; and the inability to plate isolate lands of additively produced circuits.

144. **Solder Paste**. Plating, the use of preforms, and the use of solder pastes (creams) can provide some or all of the solder needed for surface mounting. When chip carriers are involved, however, the use of solder pastes is preferred in most applicaions.

145. **Screen Printing**. Screen printing of solder pastes for surface mounting applications is basically the same technique as is used to deposit thick films on hybrid circuits. The normal screens used are 80, 100, and 200 mesh because of the large particle size. For many applicaions, the 80-mésh screen is used to deposit about 0.005 to 0.007 in. of wet paste.

146. The benefits of screen printing are many. For example, it lends itself to high-volume usage in which a uniform deposit of paste is required in intricate patterns. Also, with a good-quality paste with controlled viscosity, it is possible to

screen-print 0.006-in. high solder bumps on 0.025-in. square lands, while maintaining resolution for several hours or days.

147. **Stenciling**. The solder-paste stenciling process is basically the same as scrren printing, except that a sheet of metal with appropriate cutouts is used instead of a screen mesh. Thus, variations in the solder thickness deposited depends on the thickness of the sheet metal used.

148. **Multipoint Despensing**. An alternative method of depositing solder paste is multipoint dispensing. Such dispensing is suitable for applications requiring greater flexibility than stencil printing, such as low production runs with few chip carriers, or assemblies where the design is not fixed and device count or position vary.

149. Dispensing is also useful for the intermix of technologies, where chip carriers are to be soldered in the midst of previously through-hole soldered components. In addition, the technique may often be required for repair during the replacement of defective components.

150. **Bumped Substrates**. "Bumping" the substrate with solder is a method that supplies a sufficiently large and uniform deposit of solder for surface mounting. It consists of a stencil-printed or dispensed deposition of solder paste, followed by both cure and reflow steps before component placement. Thus, smooth solder bumps measuring 0.007 in. in height are formed. The substrate is then cleaned aggressively with solvents and brushed to remove spatter deposits, as required.

151. <u>Hot-Gas Solder Leveling</u>. The hot-gas solder-leveling process has also been considered to supply thick solder on small lands in a uniform manner due to the dominant surface tension of molten solder. However, studies have shown that thick solder, 0.005 in. typically, can be applied with this method, but the thickness standard deviation of 0.001 in. is usually unacceptable. Similarly, inconsistently thick solder can be applied to chip carrier leads by dipping.

Component Placement

152. A wide variety of equipment is being developed or already exists for the handling of surface-mounted components. Most of them are pick-and-place equipment that use a simple vacuum grid mechanism to hold the component on its placement probe. They vary in complexity from basic assembly stations to fully automatic computer controlled systems. Since the typical vacuum probe holds the component from the top and places it straight down on the substrate without the benefit of side grips, parts placement can be very dense and yet extremely accurate.

Soldering

153. Surface mounting of components places a greater emphasis on the quality of the starting materials and on process control than is required for the soldering of through-hole-mounted components. The reasons for this are many.

154. The higher packaging densities achieved and the reduced solder joint size and spacing dramatically increase the density

and total number of solder joints on the printed wiring assembly. But inspection then becomes more difficult and, thus, a more perfect job of soldering is necessary.

155. The solder joints are almost identical in appearance and spacing. The repetitious task of inspecting large numbers of geometrically identical solder joints reduces inspection efficiency, so unacceptable solder joints are likely to be over looked even after multiple inspections. To make matters worse, the defects that are found are often difficult to repair, and the repair procedure can introduce additional problems.

156. In view of these considerations, the most cost-effective production soldering processes are those that ensure acceptable quality levels through in-process control and sample-lot inspection. Therefore, acceptable quality must be guaranteed by the specification of proper (solderable) components and materials and by using soldering processes that are readily controllable.

Inspection

157. The smaller features sizes and tighter tolerances associated with high-density surface mounting applications require increased inspection and process control. For example, to prevent layer misregistration and drilling inaccuracies, optical pattern-recognition/digital image processing and comparison equipment is emerging that will allow cost-effective inspection of every layer of a high-density multi-layer board. Hole sizes, missing or extra holes, conductor widths/spacings, and open/short circuits can also be detected by such systems.

Modifications and Repairs

158. As assemblies increase in sophistication, their modification of repair becomes more complicated and expensive. Also, the possibility increases that technician errors may cause irreparable damage to the components or substrate. With these considerations in mind, improved on-site repair tools have been developed for surface-mounted components.

159. Essentially three types of problems exist on surface-mounted chip carrier assemblies :-

(a) defective components

(b) misaligned components

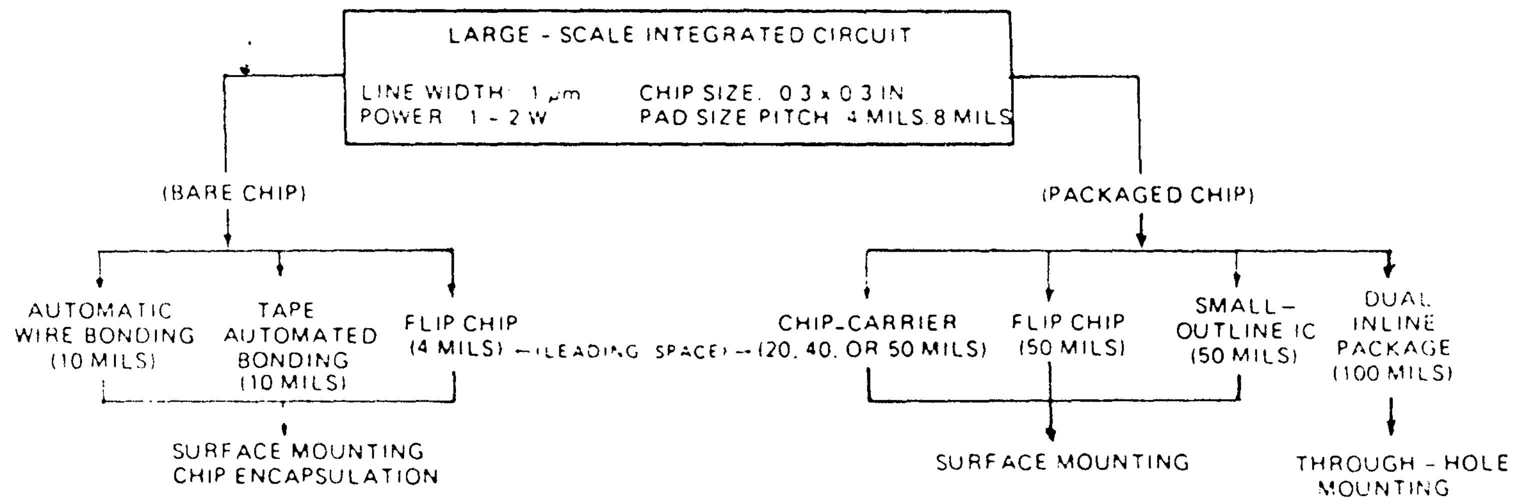
(c) incorrect conductor routing

160. To facilitate correcting each of these problems, the aisle width between components should be wide enough to facilitate inspection/testing and the making of changes.

CHIP-ON-BOARD TECHNOLOGY

General

161. There are several different ways to package and assemble integrated circuits (ICs) on printed wiring boards (Fig 27). Yet, except in hybrid circuits, IC chips have been used almost exclusively in packages supplied by the IC manufacturer. However, during the past several years, bare IC chips have begun to be used, both singly and in multiples, on printed wiring



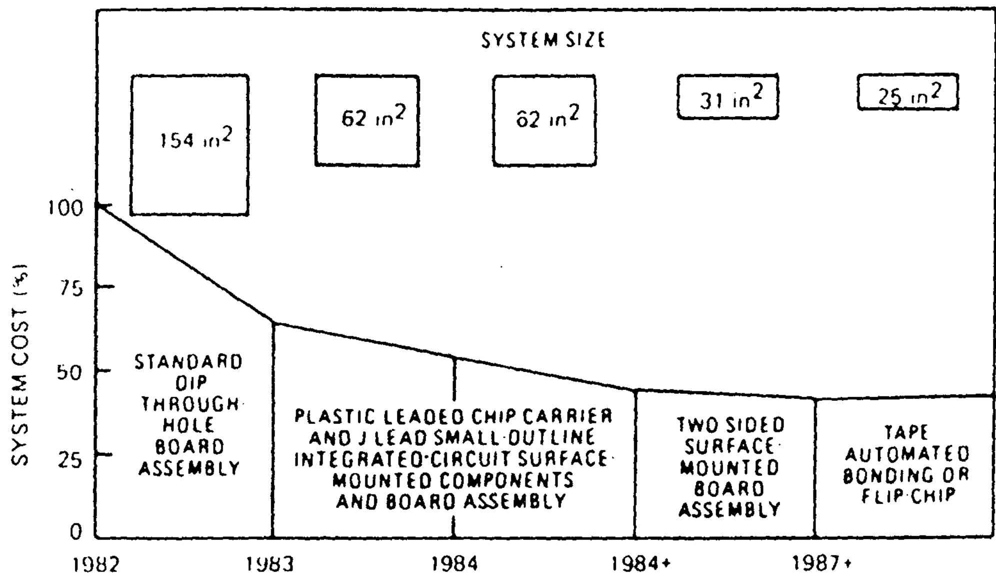
INTEGRATED CCT PACKAGING AND ASSEMBLY OPTIONS

FIGURE - 27

boards in what is referred to as chip-on-board (COB) technology. The factors that lie behind the increasing interest in COB include size, cost, semiconductor technology, encapsulation, and automation.

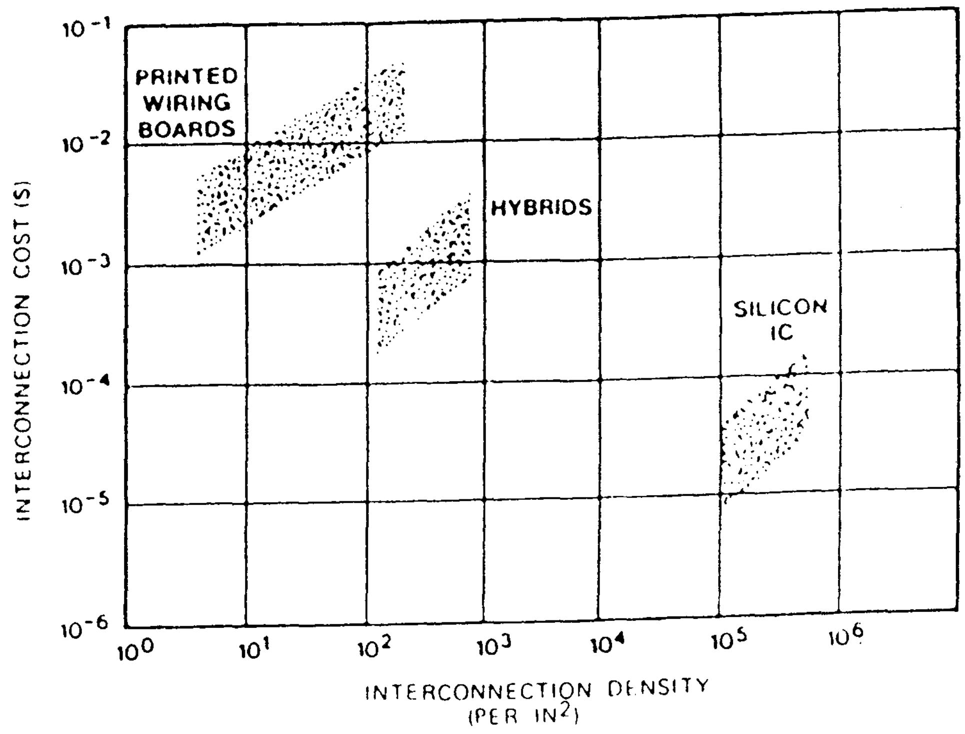
162. <u>Size</u>. The benefits of using COB all stem from the absence of the IC package. A wire-bonded chip takes up about a quarter of the area of a dual-inline package (DIP) and is also more space-efficient than leadless chip carrier (LCC) packages. Also, with a lower profile, COB can be used in applications not possible with the other packaging methods (such as in "smart" credit cards). As an example of both size and cost benefits that can be obtained with COB technology, Fig 28 shows a memory board's progressive reduction in size (and percentage of overall system cost) as it is changed from conventional through-hole (DIP) technology to surface-mounting (LCC) technology and, finally, to COB technology.

163. <u>Cost</u>. As just mentioned, lower overall system cost is another factor behind the selection of COB technology. A similar consideration relates to the fact that the cost of making circuit interconnections is much less when they are made directly on the IC chip, as opposed to making the interconnections on a higher-level packaging scheme, as shown in Fig 29. Therefore, the trend has been towards having more sophisticated IC chips. This, unfortunately, has been associated with the need for more input/output terminations and more sophisticated packages for the integrated circuit, such as LCCs and pin-grid array (PGA)



PACKAGING TECHNOLOGY COMPARISONS

FIGURE - 28



INTERCONNECTION COST VS DENSITY

FIGURE-29

packages. However, since COB technology eliminates the need for the chip package, it also avoids the cost of the expensive package and custom tooling that is often required.

164. **Semiconductor Technology**. Trends in semiconductor technology have also paved the way towards COB technology. Low-power CMOS devices, already taking a major share of the IC chip market, are ideal for the power-limited COB technology. And the trend toward custom and semicustom ICs should mean additional importance for COB.

165. **Encapsulation**. Reliability has improved with the devolopment of encapsulating materials that more closely match the thermal expansion properties of conventional printed-wiring board materials. In the part, the expansion mismatch between the encapsulant, usually a "glob" of epoxy and the board would excessively stress the joint between the chip and the board. However, recent developments with improved sealants have reduced the significance of the problem, making COB attractive for use in more applications.

166. **Automation**. Companies that have had limited results competing in lablor-in-tensive assembly markets may pay more attention to COB, as many, if not all, of the processes involved can be automated.

Semiconductor Dice (Chip) Types

167. **Back-Bonded Chips**. Back-bonded chips comprise components that are traditionally installed in discrete packages. In

transistors, for example, the bottom of the chip serves as the collector and metal pads serve as the base and emitter. The chip's collector is bonded directly to the mounting substrate, and discrete connections are made to the base and emitter. For COB applications, chip-and-wire technology is ideally suited for use with back-bonded chips.

168. The use of back-bonded chips has several advantages :-

(a) **Availability**. Nearly every IC available in discrete-package form also comes in chip form.

(b) **Size**. The small size of back-boned IC chips allows for very high packaging densities.

(c) **Heat Transfer**. The bottom of the chip dissipates most of its heat. Since in COB technology this surface is in intimate contact with the board, metallization on the board can be used as a heat sink.

(d) **Cost**. Because back-bonded chips require no additional processing by the IC manufacturer, they cost less than face-bonded chips.

169. The use back-boned chips also has some disadvantages :-

(a) **Handling and Testing**. The chip's small size makes it very difficult to handle. A few chips are usually lost during the chip-to-board transfer. Also, the tiny dice are difficult to test and attach.

(b) **Fragility**. Exposed bonds make the completed interconnection susceptible to handling damage.

170. **Face-Bonded Chips**. Face-bonded chips are dice with supplementary features that provide access to the input/output pads. For COB applications, common forms of these components include beam-tape (TAB) devices and flip chips.

171. The advantages of face-bonded chips include the following :-

(a) **Mounting**. Bonding circuit connections to metallization accomplishes both mechanical mounting and electrical interconnection in one step. It also accommodates semiautomated bonding operations.

(b) **Ruggedness**. Because the chips are somewhat enclosed, the resulting assemblies are more reliable than those using back-bonded components.

(c) **Inspection**. With some of these devices, it is readily possible to check for proper bonding.

(d) **Pretest and Burn-in**. Face bonded chips can be readily pretested for critical circuit parameters. They can also be subjected to preassembly burn-in.

172. However, the use of face-bonded chips does have some disadvantages :-

(a) **Availability**. Relatively few semiconductor components come in face-bonded chip form.

(b) **Inspection**. Some face-bonded components, such as flip chips, do not readily facilitate the inspection of the bonded interconnections.

(c) **Cost**. Face-bonded components cost more than back-bonded chips because they require extra processing by the semiconductor manufacturer.

(d) **Heat transfer**. Face-bonded components dissipate heat poorly to the board, as the only connection to the substrate is through the chip leads.

Printed-Board Considerations

173. **Layout Guidelines**. The layout of a board for COB applications, as with conventional designs, begins with the positioning of components and the routing of conductors. A prime factor that should be kept in mind is that exact placement of components is not always possible. Therefore, a good layout for volume production should be relatively immune to variations in part placement. Ideally, discrete parts should be able to be mislocated by up to 0.010 in. and up to 10 degree in rotation. Refer Table 13.

174. **Board Substrate Materials**. The selection of an appropriate board substrate material depends a gereat deal on the cost trade-offs associated with the end-product applicaion and the type of COB technology being employed. For most low-cost applications, where thermocompression wire bonding is not used, conventional printed-wiring board materials are sufficent.

TABLE - 13

GENERAL CHIP ON BOARD DESIGN GUIDELINES

Guidelines	Reasons
Die-to-Board Attachment	
Chip attachment land should be at least 0.020 in. larger than the die size on all four sides	To allow sufficient tolerances for the chip attachment adhesive and die placement during assembly
Multichip to Board Attachment	
The location of multiple chips on the board should be equally spaced and on the same axis	To simplify die attachment, wire/lead bonding, and encapsulant/cover placement automation
Lead Bonding	
The bonding land on the board should be at least 0.020 in. from the chip attachment land	To avoid bridging of the chip attachment adhesive
The width of the wire/lead bonding land on the board should be at least 0.010 in. The bonding area should be at least 0.010 in. × 0.030 in.	To allow sufficient area for bond placement and rework
Bonding Wire/Lead	
The length of the bonding wire/lead between the chip and board lands should not be greater than 0.100 in.	To minimise wire/lead sagging
Spacing between adjacent wires/leads should be a minimum of 0.010 in.	To avoid shorts
The tip of the bonding wire/lead should preferably have a square configuration	To enable easier judgment of the reference points taken during automatic wire/lead bonding
Solder Mask	
The solder mask opening should be at least 0.050 in. from the edge of the bonding lead	To avoid bond placement on the solder mask

175. Where thermocompression wire bonding is employed, consideration must be given to the high temperatures associated with this process. When cost is an overriding consideration, localized bond-site charring and delamination are often tolerated when conventional board materials are used. However, when this is not allowed, special high-temperature epoxy/glass and polyimide/glass board materials are often used.

176. For special COB applications, the use of flexible printed-wiring, conductive-polymer, and molded-thermoplastic board materials has also been considered.

Chip Attachment

177. Chip Handlers. The chip-on-board assembly industry has now begun to closely follow similar manufacturing methods and procedures of those already well established in the semiconductor and printed circuit industries. However, due to the realtively small size of this market and the associated geometric complexities, which necessitate extermely accurate placement of the chips, there has been a slower rate of progress in automating COB chip-handling operations.

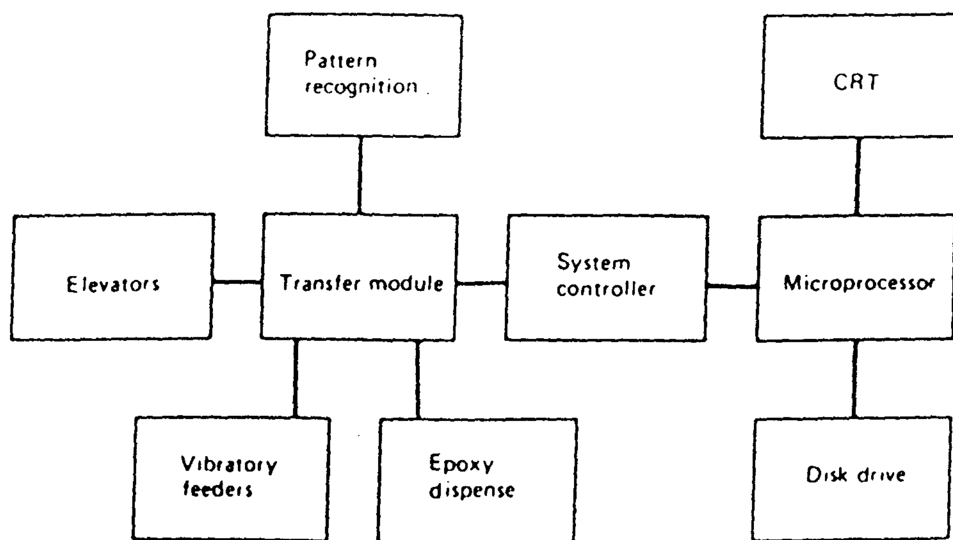
178. Low-Volume Equipment. With this in mind, various approaches have been taken to solve COB manufacturing problems with cost-effective solutions for the particular applications involved. A typical approach for low-volume applications combines proven technical components that have been used for computer graphics

with system components that have been developed for front-end semiconductor manufacturing.

179. The basic system (Fig 30) consists of a transfer module and a controller. The system controller provides the interface and control electronics; the transfer module is where the assembly actually takes place. This particular system has been adapted from a flatbed plotter with an 11-in. x 16-in. work area that can be used with many combinations of input and output fixturing.

180. Virtually any type of semiconductor device can be handled by equipment such as this, with chip dimensions ranging from 0.020 in. to 0.300 in. Several collet stalls are used to hold collets of varying size, so that several combinations of chip sizes can be programmed in a single assembly operation. A vacuum force is typically used to pick up the chips, thus eliminating distortions or scratches from mechanical fingers. A vacuum-sensing circuit is also often used to detect if a device was picked up and transported correctly. If no device is sensed, the operator has the option to continue, retry, stop, or skip to the next chip.

181. Once the part has been picked up by the collet, it is placed on the centering nest and squared. The motorized centering nest has a programmable ratational capability that is adjustable in 1.8 degree increments.



COB CHIP HANDLING SYSTEM BLOCK DIAGRAM

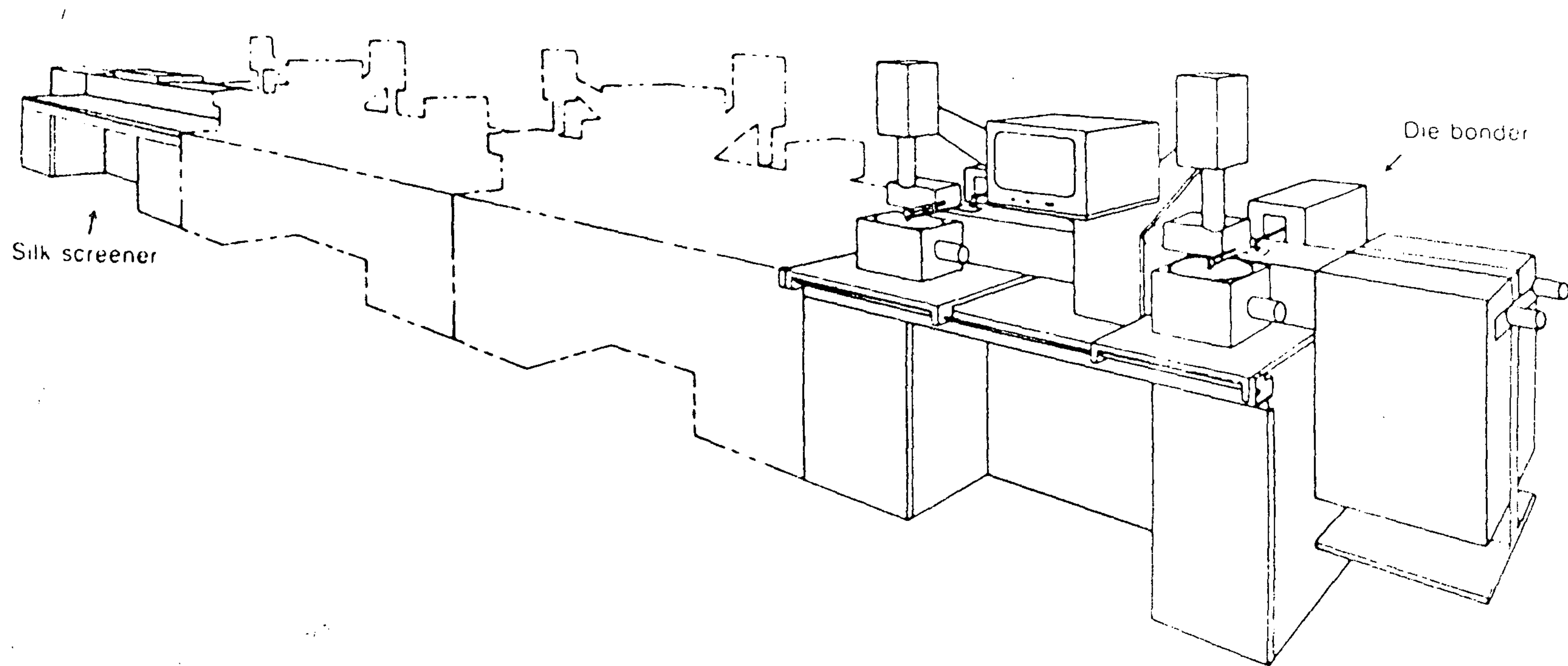
FIGURE-30

182. The more sophisticated units have a pattern-recognition feature that is performed by a camera system mounted directly over the centering nest. The orientation is then electronically compared with stored images, and the device is turned to the correct orientation. The chip can now be turned to the proper angular alignment, picked off the nest, and placed onto the board. The motion is also programmable to control chip placement pressure. With a system such as this, throughputs of up to 1200 chips/hr can be realized.

183. <u>Fully Integrated Systems</u>. High-volume, fully integrated systems are also being developed for multichip applications. A typical system (Fig 31) processes up to 12-in. x 12-in. boards in 50-unit magazine equipment.

184. A fully integrated system could be configured to include equipment for adhesive silk screening, pick-and-place die attachment, wire/lead bonding, and chip sealing. Such a system would operate in the following manner. First, bare boards located in 50-unit magazines are presented to the input feed magazine of the silkscreener, where adhesive is deposited. Then the boards with adhesive are automatically transferred to the pick-and-place machine, where the chips are placed on the board over the adhesive. The populated boards are then put back in the magazine for further processing.

185. The magazines are removed from the output of the chip attachment unit manually and put into an oven to cure the adhesive. The boards, after curing in the magazines, are put



FULLY INTEGRATED CHIP ON BOARD ASSEMBLY SYSTEM

FIGURE 31

into the wire/lead bonder's magazine feed. The chips are then bonded to the boards and automatically put back into the magazines. These magazines are placed manually into another wire/lead bonder for inspection and repair.

186. The inspected magazines are then taken to the chip-sealing unit. The boards are environmentally sealed and returned automatically to the magazines. These sealed units are then taken to another oven for curing of the sealing compound.

187. If more sophistication is desired, a control console can be added to oversee the operation of the system, consisting of a closed-circuit television monitor, a keyboard, and a tracking assembly that allows an operator to intervene by remote in the operation of the equipment.

Chip Bonding Adhesives

188. Depending on the COB wire/lead attachment method being used, it is often necessary to attach the chip to the board with an adhesive. The better-known general types of adhesives are listed in Table 14.

189. Epoxy. Because of their superior properties, conductive and nonconductive epoxy bonding methods are usually best for attaching chips to boards (They also rival passive chip solder bonding).

190. In conductive epoxy bonding, metal particles (usually silver or gold) are added to the basic epoxy resin. When the resin

TABLE - 14

CHIP BONDING ADHESIVE TYPES

Type	Advantages	Limitations
Phenolics	Very high bond strength	Used mostly for structural applications, possibly corrosive, difficult to process at low temperatures
Polyurethanes	Easy to rework	Not suitable for temperatures above 120°C, relatively high outgassing, some decomposition
Polyamides	Easy to rework	High moisture absorption, high outgassing, variations in electrical insulation properties, especially when exposed to high humidity
Polyimides	Very high-temperature stability	High cure temperatures, require solvents as vehicles
Silicones	High-temperature stability, easy to rework, high purity, low outgassing	Moderate to poor bond strength, high coefficient of thermal expansion
Epoxies	Some are easy to rework by thermomechanical means, some are low outgassers, easy to process, can be filled to 60-70% with a variety of conductive or nonconductive fillers	Depending on type of curing agent used and degrees of cure: outgassing, catalyst leaching, corrosivity
Cyanoacrylates	Very rapid setting ($\approx$10 sec) give very high initial bond strengths	Bond strengths often degrade under moist or elevated temperature ($\leq$150°C) conditions

cures, the metal particles remain in contact in suspension and thus provide electrical connectivity and thermal conduction. Nonconductive epoxies, on the other hand, contain a basic resin or incorporate additives to promote heat dissipation.

191. Epoxies designed for use with bare chips do not contain volatile solvents. Also, because they do not significantly outgas, even at high temperatures in a low vacuum, they can be used to bond chips to boards without forming voids between them.

192. Epoxies have several other advantages, including :-

(a) <u>**Low Temperature Cure**</u>. Most epoxies cure near 150 degree C. This low temperature does not degrade the electrical properties or the reliability of the chips, as do some other bonding methods.

(b) <u>**Ease of Processing**</u>. Epoxy bonding equipment is straightforward to use. In many instances it can be deposited on all designated board areas simultaneously with the same silk screening equipment as is used for processing the board itself.

(c) <u>**Ease of Handling**</u>. It is possible to store boards containing wet epoxy for a long time before mounting the chips.

(d) <u>**High Yield**</u>. Devices bonded with epoxy exhibit yields approaching 100%.

(e) **Ease of Repair**. After the epoxy heats to its softening temperature, it is easy to remove a faulty chip and replace it with a good one.

(f) **Ruggedness**. An epoxy bond's mechanical strength is sufficient to withstand most rough handling and most shock and vibration environments.

193. As with other chip mounting processes, epoxy bonding involves trade-offs. In particular, its use dictates that certain precautions be taken, including :-

(a) **Heat Control**. When thermocompression wire bonding is used, a bonder with a heated probe tip must be used, as the heat associated with some types of thermocompression wire bonding will soften the epoxy. (However, this precaution does not apply when thermosonic wire bonding is used).

(b) **Precision Tools**. If a vacuum-hold chuck is used to mount the chips, each component should be checked to be sure that a positive seal forms against the probe tip. Otherwise, the epoxy might be drawn to the top of the chip.

(c) **Chip Processing**. Sinter semiconductor chips have gold backing in order to alloy the gold with the silicon. If the gold is evaporated, the epoxy can pull it away from the chip and form a high-resistance contact.

194. **Polyimide**. The use of polymides and silver-filled glass adhesives in increasing due to their lower containing

approximately 70% silver powder in a polyimide resin that has been dissolved in a high-boiling solvent.

195. To minimize the quantities of solvents and other vapors released during cure, the polyimides used in chip attachment adhesives are low-molecular-weight resins that cure by an addition reaction. They are supplied and used in much the same way as the epoxies.

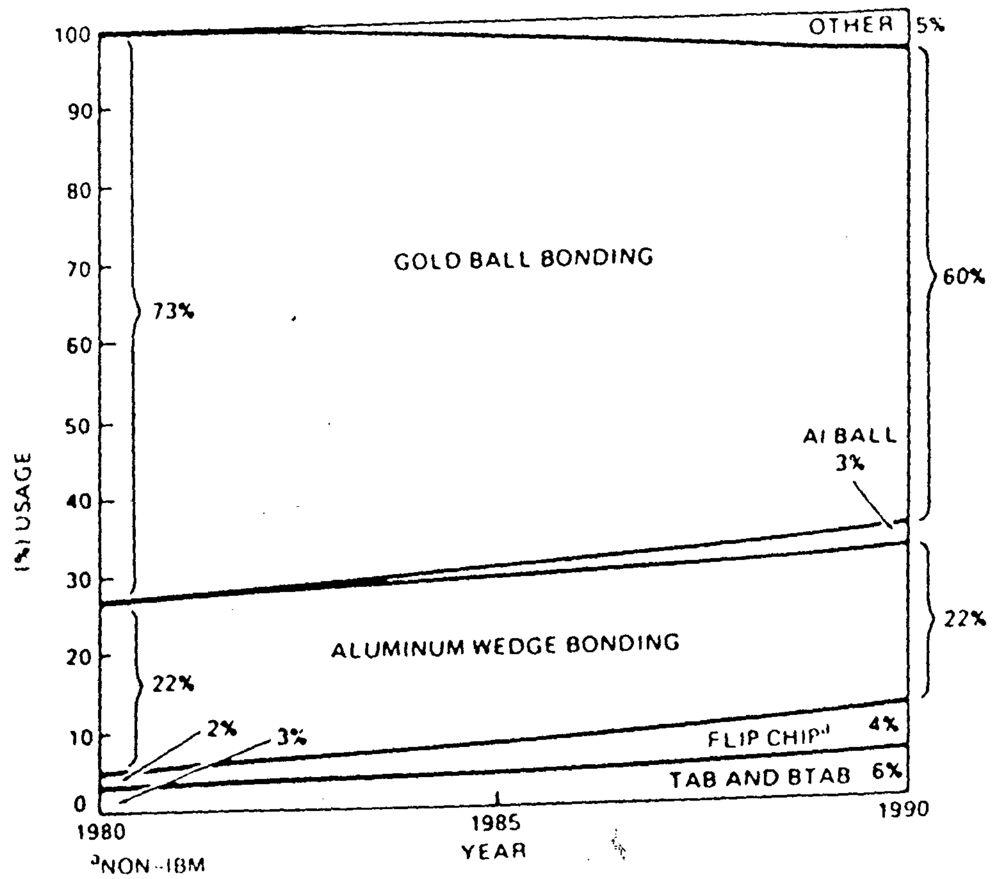
196. The main objection to their use is that they are organic polymers and it is difficult to remove all of the organics. If all the organics are not removed, they may outgas and cause chip degradation.

Chip Termination Techniques in General

197. The three basic chip attachment and termination techniques, or derivatives thereof (Fig 32) wire bonding (chip -and- wire), tape automated bonding (TAB), and controlled-collapse (flip-chip) bonding-have been used in some cases for over 20 years in semiconductor packaging and in hybrid assemblies. All of these techniques have been refined to the point where they are suitable for COB applications.

Chip and Wire Technology

198. Chip and wire technology is commonly used in COB applications to make the majority of interconnections between the IC chip and the board. Unlike some of the other COB technologies, this technology requires the COB assembler to make two bonds per



CHIP TERMINATION TECHNIQUES

FIGURE - 32

chip interconnection. There are three basic types of wire bonding :-

(a) Thermocompression. Thermocompression wire bonding uses a combination of heat (Approximately 270'C) and compression to connect the wire to the IC chip and to the board. The basic method actually encompasses three different bonding processes: ball, stitch, and wedge.

(b) Ultrasonic. Ultrasonic wire bonding relies on a wire-to-conductor land interface's mechanical resonance to absorb the energy needed to weld the wire to the land. An ultrasonic oscillator generates the resonant frequency.

(c) Thermosonic. Thermosonic wire bonding heats the substrate to 150'C and uses ultrasonic energy to provide the remainder of the energy required.

199. By the time a chip reaches the interconnection stage of assembly, a considerable investment has been made in materials and labor. Therefore, high yields in these late process stages can result in greater cost savings than can be realized at earlier stages of the process. For this reason, COB manufacturers carefully follow precisely defined processing procedures, and place stringent demands on the materials and equipment used in wire bonding.

200. **Bonding Wires**. Both gold and aluminum wire are used for COB applications. The gold wire are typically alloyed with small amounts of beryllium copper to control grain growth during

bonding. Aluminum wires are typically alloyed with 1% silicon. The following factors influence the choice of bonding wire and equipment:-

(a) Maximum processing temperature, including rework.

(b) Size of the bond sites on the IC chip (0.001 in diameter wire for thermosonic ball bonding requires a land size greater than 0.0025 in)

(c) Board substrate materials.

(d) Final operating and nonoperating environment.

(e) Geometry of the board assembly, which may restrict bonding tool access.

<u>Tape Automated Bonding</u>

201. A relatively recent concept that appears to have a bright future for COB applications is known as tape automated bonding (TAB). This technique utilizes photo-imaging/etching process to produce fabricated conductors on a dielectric tape in movie-film format.

202. The most visible aspect of the TAB system is the carrier tape, which is stored on reels similar to movie film, in widths from 8 to 70mm. Windows are punched at specific locations in the tape and a thin, often 0.0014 in thick, conductive foil is bonded to the tape, which is usually either mylar or polymide. A conductive pattern is then etched in the foil to give the desired interconnection circuitry with "beam-type" leads extending over the windows in the tape.

203. In subsequent processing, the beams are simulaneously bonded to the chip, which is located precisely under the window. The exact location of the chip with respect to the sprocket holes on the tape carrier permits automated tape-handling equipment to be used that accurately positions the individual chips for the subsequent processing operations. for COB applications these include testing, burn-in, and mounting onto the board. TAB provides a means of mounting bare IC chips to printed boards with the following advantages:-

(a) The bonding areas on the chip can be bermetically sealed when a gold bump is constructed on the bonding land.

(b) Less gold is required for TAB than is needed for wire bonding. TAB provides a means for pretesting and "burn-in" of the chips prior to their final mounting on the board.

(c) Bonding lands can be as small as 0.002 in. on 0.004 in. spacing. Input/output counts can be as high as 300 or more leads.

(d) Very-;pw (0.030 in) profile COB assemblies can be made.

(e) TAB provides a method for automated (and robotic) simultaneous bonding of all the leads to the chip and to the board.

(f) The TAB process chips require only a fraction of the board surface area required for mounting packaged chips.

(g) The rectangular TAB lead provides a lower conductance than does a round wire, enhancing its use in high-speed applications.

204. The disadvantages associated with using TAB process include:-

(a) It requires specially designed equipment to match each application, at both the chip and the board interfaces.

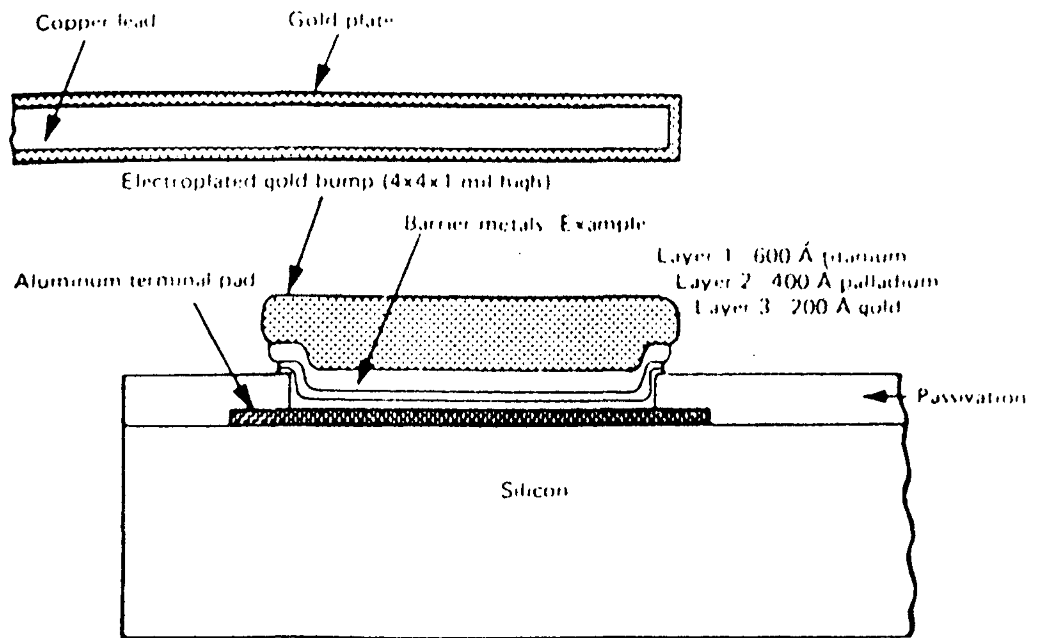
(b) In general, TAB chips cannot be purchased economically in small quantities.

(c) At present, there is a lack of commercially available "bumped" wafers of chips.

(d) TAB bonding and bumping equipment is rather sophisticated.

205. **Types of Tape Automated Bonding**. The initial stage of TAB wager preparation is much the same as that for wire-bonded wafers. A pinhole-free silicon nitride passivatgion layer or, in some cases, silicon dioxide or polyimide, is deposited at low temperatures, The passivation is selectively removed, leaving a good portion of the aluminum land exposed. The chip is now at a state where it can be presented either for wire bonding or for additional TAB fabrication.

206. **Basic (Bumped-Chip) TAB**. At this point in the preparation of a chip slated for TAB, it can be processed in one of two ways. In the basic TAB, approach (Fig 33), a barrier metal, such as



BUMPED CHIP TAB INTERCONNECTING GEOMETRY

FIGURE - 33

titanium-tungsten, is deposited over both the exposed aluminum and over the passivation on the periphery of the land. This, plus the addition of 0.001in. high gold bumps, helps to ensure the reliability of the TAB connections to the tape during the inner-lead-bonding (ILB) process.

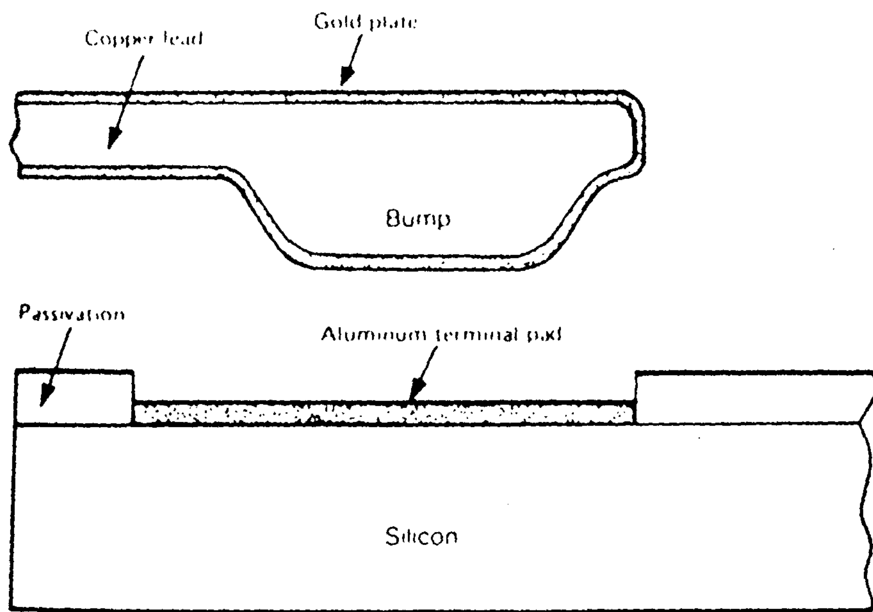
207. The bumps on the chip are electroplated onto the barrier metal at each land position. Copper bumps can also be used, and both copper and gold can be tin-plated, This completely seals the chip and, thus, further enhances TAB's reliability as a COB assembly process.

209. <u>**Bumped-Tape TAB (BTAB)**</u>. The other processing approach (Fig 34) puts the bump on the tape rather than on the chip. This approach is known as BTAB. In either case, the bumps are necessary to elevate the etched tape conductors above the chip to prevent shorting of the leads.

210. <u>**Area TAB**</u>. One of the most recent interconnection technologies is known as are TAB. In this approach, circuit patterns are fabricated on the tape. This allows the chip designer to put the I/O lands at any position on the chip, as opposed to being on the periphery of the chip. This reduces the signal path lengths required and therefore redduces signal delay.

<u>**Special Chip Configurations**</u>

211. Special chip configurations, such as flip chips and beam leads, require different bonding technologies. Flip-chip, or



BUMPED - TAPE TAB INTERCONNECTION GEOMETRY

FIGURE - 34

face-down, and beam-lead bonding utilize techniques such as ultrasonic bonding, welding, and soldering.

212. **Flip-Chip Technology**. The original flip-chip concept employed small, solder-coated copper balls sandwiched between the chip termination lands and the appropriate lands on the interconnecting substrate. The resultant solder joints were made when the unit was exposed to an elevated temperature. However, the handling and placement of the small-diameter balls was extremely difficult, and the operation was costly.

213. In a more advanced technique, a raised metallic bump or lump, usually solder, is provided on the chip termination land. This is normally done on all lands of all of the chips while they are still in larger-wafer form. The individual chip is then aligned to the appropriate circuitory on the substrate and bonded in place using reflow soldering techniques. In this way, the interconnection bonds between the chip and the substrate are made simultaneously, thus reducing fabrication costs. The primary advantages of using flip-chip packaging are :-

(a) Fast throughput times.

(b) Efficient use of board area.

214. The major disadvantages include :-

(a) The inability to inspect the assembled chip visually.

(b) The limited availability of bumped chips.

(c) Difficult flux removal.

(d) Thermal transfer complications.

215. A solution to the availability problem is found in using the approach by which the bump is produced as part of the circuitory on the interconnecting substrate, rather than as part of the chip. Thus, the COB assembler can use any of the devices that are available in bare-chip form.

216. **Beam-Lead Technology**. The other major special chip configuration is beam lead. In this technology, the lead is produced with plating techniques during the chip fabrication processing on the undiced wafer.

217. The advantages of using beam-lead devices include :-

(a) Ease of alignment of the chip to the interconnecting substrate.

(b) Its campatibility with a number of lead-bonding techniques, including soldering, thermocompression, and thermosonic bonding.

(c) When compared to wire bonding, the reduction in the number of bonds required to interconnect a chip to the substrate.

(d) The inherent reliability of the beam-lead structure due to its superior electrical, mechanical, and thermal characteristics.

218. The major drawbacks to using beam-lead technology include :-

(a) The Limited availability of beam-lead chips.

(b) The larger area required during chip processing, which means that fewer devices can be produced per wafer.

219. Special Chip Applications. The use of flip-chip and beam-leaded devices has been limited to very special packaging applications. Whether or not these can be considered to be COB applications depends on one's definition of "board," as most of the applications pertain to the use of ceramic substrates. In general, such applications have been referred to as "hybrids." These techniques have not been applied to conventional printed wiring boards to a significant degree.

Chip Protection

220. Increasingly, many applications are requiring that the COB assembly protect the chips from the atmosphere-i.e., that the chips be sealed, hermetically when practical. The means for doing this fall basically into two categories, "glob-top" coatings and lids.

221. In selecting the technique to be used for the seal, several important properties must be considered :-

(a) Sealing Temperature (and time). The technique chosen must be able to form a seal at a low enough temperature and in a short enough time so as to minimize the heating effects on the chip and board components.

(b) Thermal Expansion. The thermal expansion of the sealing material/device should also closely match that of

the board in order to minimize thermal stresses and thus maintain the integrity of the seal.

(c) **Hermeticity**. The seal must provide the degree of hermeticity required and maintain this level when exposed to the equipment operating and storage environment.

(d) **Cost**. The sealing technique must be cost-effective, not only with respect to material cost, but also with respect to application and replacement costs, when applicable.

(e) **Repairability**. If it is necessary to be able to replace a chip or repair a wire/lead termination after the chip has been sealed, it is important that th e seal can be readily "broken" and replaced.

(f) **Stability**. When coatings are use, they should be sufficiently stable that they do not tend to excessively stress the wire/lead bonds or and die attachment bond when exposed to the equipment operating and storage environments.

222. **Protective Coatings**. The protective coatings are as follows:-

(a) RTV Dispersion Coating. Typical RTV dispersion coatings are one-component, room-temperature-vulcanizing (RTV) silicone rubber coatings supplied as xylene disperson. The curing process uses a cross-linking mechanism that generates methanol during cure. Once applied and exposed, the material

vulcanizes by reaction with moisture from the air to form a soft, resilient elastomeric coating, which will withstand longterm exposure to temperature as high as 250°C.

(b) Silicone Dielectric Gel. Special controlled technology can yeld a silicone gel that affords the nonflowable permanence of a soled, but also gives the freedom from large mechanical and thermal stresses of a fluid. Chemically, a typical silicone gel is very similar to a silicone fluid, but with just enough cross linking to prevent separation of the individual polymer chains and give nonflow thermal-set properties. The fully cure dielectric gel is a soft, jellylike material that exhibits tenacious pressure sensitive adhesion to virtually any substrate,

(c) Epoxy Coatings. Epoxy coatings are also available for COB self-crowining or "glob top" applications. Typical materials are two component, liquid epoxy/anhydride systems that have been formulated for their superior thermal shock performance, substrate adhesion, moisture resistance, and glass-transition temperatures in the range of 165-180°C.

223. Traditionally, the differences among printed-board assemblies, hybrid circuits, and integrated circuits have been related to base materials that are used, i.e., organics, ceramics, and silicons, respectively. However, using the base material as a determining factor no longer seems to be appropriate, due to the wide range of material combinations now being used in the electronics packaging and interconnection industry.

224. In general, the characteristics of all electronic circuit assemblies can be viewed as being application-specific. Thus, if their base materials are not considered, it is possible to define new categories of electronic circuit assemblies. In this view, the hierarchy of electronic circuit packaging elements is as follows :-

(a) Printed-board assemblies (application - specific electronic assemblies)

(i) Usually larger than 10 in.2 in base size.

(ii) Usually provide interconnection for packaged components, both through-hole and surface-mounted.

(iii) Usually use copper foil/plating as the primary interconnection wiring.

(iv) Use various base materials, including nonorganic or ceramic materils with or without reinforcements, constraining cores, or supporting planes.

(v) May also provide mounting for unpackaged semiconductors, which are subsequently protected by an individual coating and/or cover.

(b) Multichip modules (application-specific electronic sub-assemblies)

(i) Usually less than 10 in.2 in base size.

(ii) Usually provide interconnection for surface-

subsequently protected by an overall coating and/or enclosure.

(iii) Usually use thick-and/or thin-film passive components and interconnection wiring.

(iv) Usually interconnected and mounted on a printed-board assembly

(v) Usually use either ceramic or silicon base materials

(vi) Contain more than one discrete active (integrated circuit) device.

(c) Integrated circuits (application-specific electronic components)

(i) Usually 1 in. 2 or less in size.

(ii) Consist of several active circuit devices and interconnection wiring, usually made simultaneously by bipolar or metal-oxide semiconductor (Tr) fabrication processes.

(iii) Base material usually silicon glass (or gallium arsenide), sometimes enhanced nby other materials.

(iv) Usually mounted and interconnected in a printed-board assembly (packiaged) or multichip module (unpackaged).

(v) When packaged, usually protected by a permanent inseparable coating or encapsulat.

Although these descriptions are not perfect, they do provide a basis for defining the variations in using these products in different applications.

MICROMINIATURE MULTICHIP MODULE

General

225. Future electronic packaging needs will increasingly emphasize the speed and density of interconnections. However, conventional printed board assemblies and integrated circuit paackages rely heavily on interconnnections of dimensions that are much larger than those encountered on the integrated circuit chip. A great deal of performance is therefore sacrificed in these external signal paths.

226. External paths are not the only cause of loss of performance. Since the percentage of the semiconductor substrate area in conventional board level packaging can be as low as 5% the combined effect relatively large external connections and low active component density is substantial.

227. In addition, if one examines the paths typically found in multiple plug-in printed-board assemblies, another cause for loss of performance is identified. Wires must be routed with some length of connection on the backplane. Although the volume density for such multiple plug in board systems is sometimes

fairly high, the use of connectors imposes limitations omn the signal paths that prevent the achievement of maximum practical density.

228. Also, much of current technology is motivated by mechanical requirements for assembling and repairing multiple integrated circuit assemblies. Therefore, future performance improvements can be obtained only by adapting this circuit partitioning and repair strategy to finer-pitch dense wiring or by modifying (abondoning) the repairability requirements altogether in interest of speed.

229. Microminiature multichip modules are (Table 15) are attractive for these system applications where interchip delays are critical to performance. The use of microminiature multichip modules is also attractive. for those applications where a functional unit can be clearly defined.

230. Fortunately, the level of development activity directed toward microminiature multichip module packaging is increasing. As will be shown, new substrate materials are being investigated, including silicon wafers. Both organic and inorganic materials are being evaluated as dielectric layers. Fine-line lithography is being used with thin film metallization, either aluminum or copper, to fabricate circuits with 10 micro meter feature sizes.

<u>Data Processing Application</u>

231. Faster machine cycle time has always been a major objective in designing computers. from the standpoint of hardware

TABLE - 15

GENERAL MICROMINIATURE MULTICHIP MODULE PARAMETERS

Technology	Number of chips	Number of I/Os	Number of transistors[a] ($\times 10^3$)	Area (mm^2)	Chip area fraction[b] (mm)
Mitsubishi HTCM	9	624	108	66 × 66	0.13
Hitachi RAM	6	108	?	27.4 × 27.4	0.06
Honeywell SLIC	110	240	?	80 × 80	?
NEC SX	36	2177	144	125 × 125	0.15
IBM 4381	36	882	252	64 × 64	0.19
IBM 3090	100	1800	600	150 × 150	0.10
NTT	25	900	?	85 × 105	0.18

[a]Based on an average of four transistors/gate.
[b]Chip-to-module area ratio.

implementation, it is therefore important to place as many logic gates and memory devices in as close proximity as possible. Thus, the challenge in designing and manufacturing general purpose computers is to achieve these goals while offering a good cost/performance ratio and flexibility for various applications.

232. The various packaging approaches taken by some of the major large-scale, general-purpose computer manufactureres (Table 15) reflect the abilities of each manufacturer at each electronic circuit packaging level. As shown, IBM, Hitachi, and NEC take the traditional three-package level approach, although there is a difference in where middle level printed board assemblies and microminiature multichip modules are used. Fujitsu, on the other hand, eliminates the middle packaging level altogether in its system.

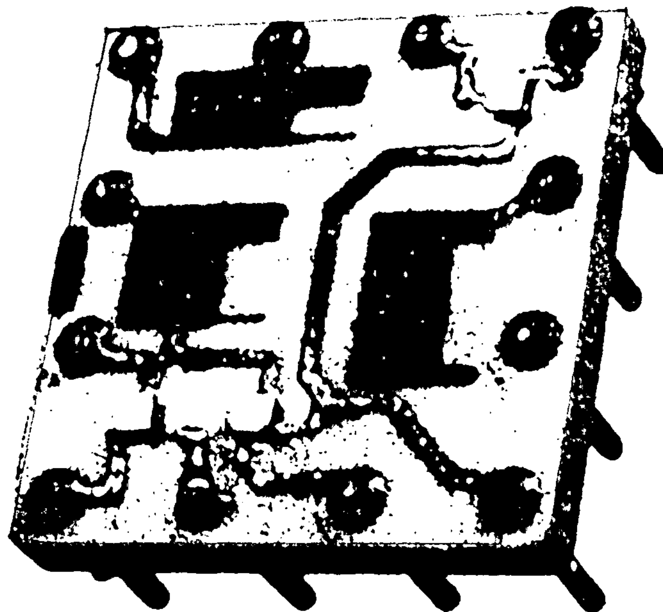
233. Common to all the computer systems in Table 15 is the use high pin count emitter coupled logic (ECL) devices, which operate with subnanosecond switching time. when in full operation, these ECL devices emit an enormous amount of heat. So, from the very beginning, thermal management considerations, are a very important aspect of hardware design.

234. The bottom line seems to be where to concentrate interconnections and support hardware. The question is, then, whether a selected configuration can be manufactured, and if so, whether it iscost effective. The following descriptions of the technologies used by each company should shed more light on this subject.

235. <u>IBM Multichip Module Technology</u>. In 1964 the IBM corporation systyem 360 introduced a new kind of circuit package called solid logic technology (SLT). Each SLT package, or multichip module, consisted of up to four single transistor chips and screen-printed thickfilm resistors mounted on a 0.5 in.2 alumina ceramic substrate (Fig 35). The 0.015 in. transistor chips were attached flip chip fashion face down with three 0.0005 in diameter copper balls, which also provided a path for heat dissipation, These balls were soldered to thick-film conductors that fanned out to the module pin connections. Twelve to sixteen module pins were available for connection to the next higher level of packaging, forming the begninning of the pin-grid array PGA package.

236. In 1969 IBM introduced a newer packaging technology called the monolithic systems technology MST. The chips had become larger and now averaged six to seven circuits per chip, requiring 16 terminations, though MST chips with up to 25 circuits and 19 terminals were also used.

237. The increased chip size created problems with respect to solder joint failure (due to coefficient of thermal expansion mismatch) and reduced productivity (due to the complexity of placing more copper balls). IBM's solution to these problems was called the controlled collapse chip connection, or c-4 technology replaced the copper balls with a lead-alloy pad. Surface tension of the molten solder joint aligned the chip on the substrate and created a strong interconnection.



SOLID LOGIC TECHNOLOGY

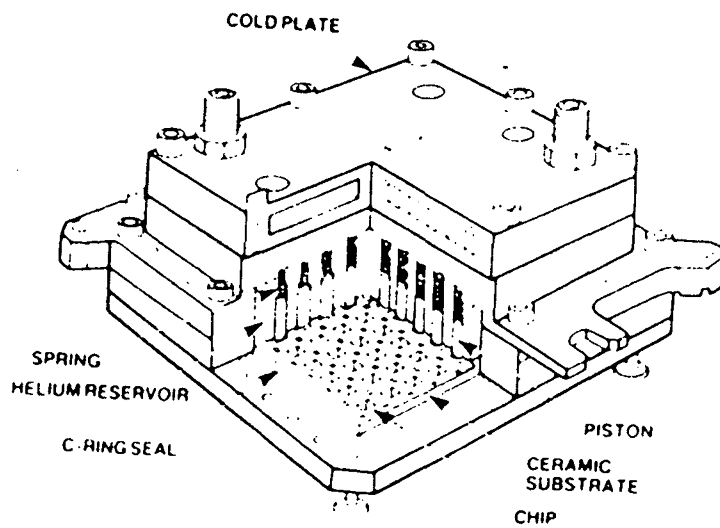
FIGURE - 35

238. The 121 c-4 chip to substrate interconnections were arranged in an 11X11 array on 0.25 mm centers. The back side of the 50 mm square MCM was populated with 361 I/O pins in a 19X19 array on 0.25 mm centers; the 35 mm square MCM had 196 I/O pins in a 14X14 array. These large pin-grid arrays were then mounted and interconnected by multilayer printed-wiring boards.

239. A typical 50 mm square MCM contains six LSI logic chips utilizing a total of 4000 circuits. This corresponds to the circuit count of 18 fully populated printed-board assemblies in an IBM Syste,/370 Model 148 computer. Thus, in a grand leap from its predecessors, essentially simple space savers, the MCM provided most of the signal and power distribution that was conventionally accomplished on printed wiring boards.

240. The culmination of c-4 packaging technology evolution came about in the early 1980s with the development of the thermal conduction module, or TCM (Fig 36) which is the heart of the high perfomance, liquid cooled IBM 3081/3090 processors. The TCM holds up to 133 high-performance bipolar LSI chips and dissipates up to 300W, permitting the circuits to operate at full potential by removing certain limits on signal and power distribution and thermal dissipation.

241. <u>Fujitsu M-70 Packaging Technology</u>. Before proceeding with descriptions of the microminiature multichip module packaging technologies being used by other electronics companies, let us look at an alternative approach. For example, the Fujitsu, Ltd.



THERMAL CONDUCTION MODULE

FIGURE - 36

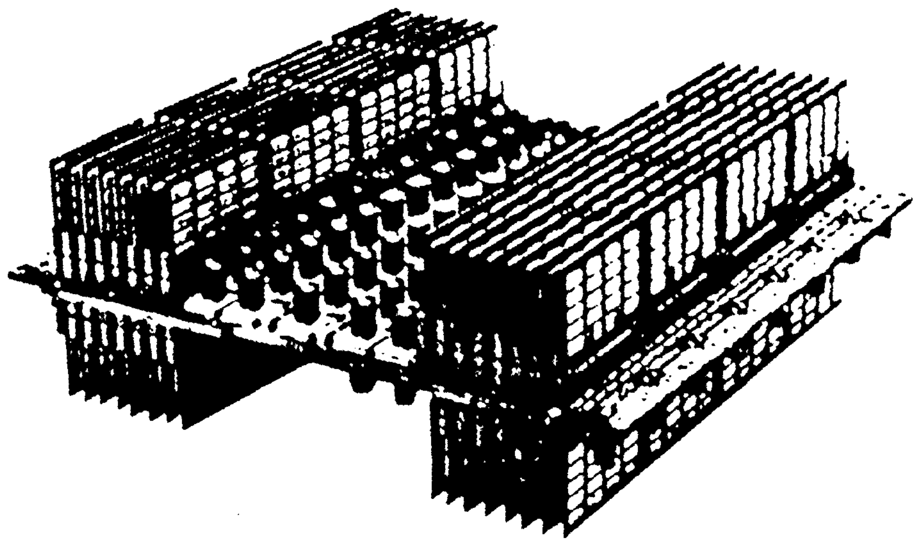
M-70 central processing unit is built entirely with surface-mounted, packaged integrated circuits.

242. Also the M-780's main storage unit includes a horizontal motherboard with up to 32 vertically stacked plug in daughterboards, each of which can contain up to 128 megabytes of memory (Fig 37). Other main modules, the memory control unit and channel processor, are packaged as single multilayer printed board assemblies.

243. **Hitachi Packaging Technology**. Another example of high density, high speed surface mount technology is used in the Hitachi Ltd. M-68X computer. The logic section of M-68X consists of a printed board assembly that mounts and interconnects 72 LSI fal packs, either bipolar gate arrays or memory modules. Its 419 mmx 280 mm polyimide glass multilayer board has a total of 20 layers ofinterconnection 2 surface layers, 8 signal layers, and 10 power and ground planes.

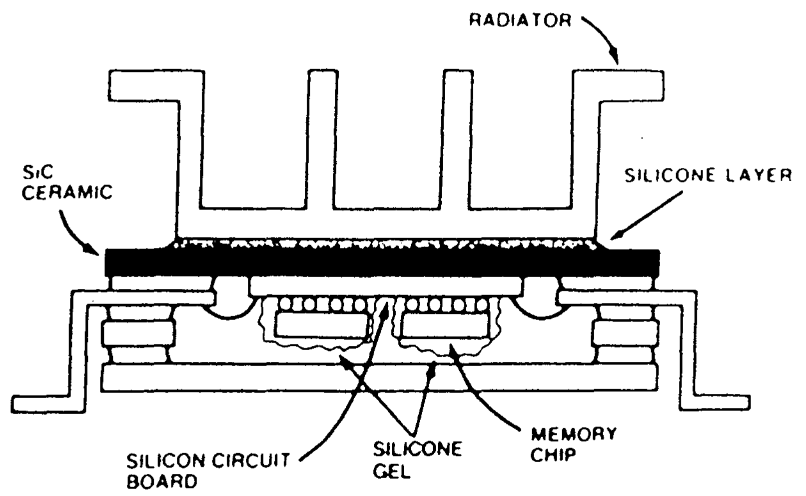
244. The 2000 and 5000 gate array packages are 22 mm square in size and have 160 I/O leads, 40 on each side, with a lead pitch of only 0.5 mm. Cache memory modules are in 29 mmx 39mm ceramic flatpacks with two rows of 48 leads on 0.75mm centers. Proprietary laser relflow soldering is used to make the nearly 20,000 connections between the flatpacks and the multilayer board.

245. Hitachi also uses microminiature multichip modules in its S-810 array processor for large scale scientific applications. In



MAIN MEMORY STORAGE UNIT

FIGURE - 37



MICROMINIATURE FLATPACK MULTICHIP MODULE.

FIGURE - 38

this computer the memory chips are packaged in 31mmx29mm flatpacks that have a silicon carbide (sic) ceramic base. The 16mm high RAM multichip modules (Fig 38) have 108 I/O gullwing leads.

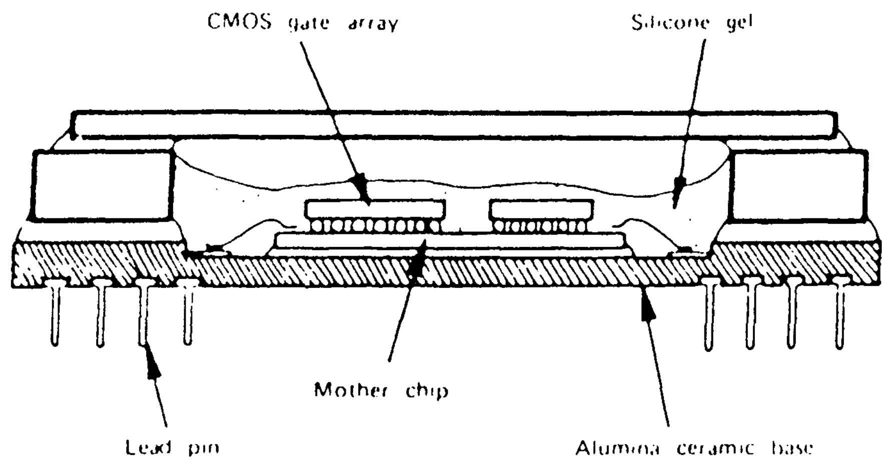
246. A relatively large silicon "mother chip" is bonded to the module's SiC base. Then up to eight 1 W ECL 1.9mmx4.0mm chips are "solder bump/flip chip" reflow-soldered to the mother chip to interconnect the memory circuits.

247. A silicone gel is used to encapsulate the bare chips within the module, to protect them from humidity and alpha particles, before a final protective cover is attached. A finned aluminum heat sink is attached to the reverse side of the SiC base with a 50 micrometer thick conductive silicone rubber adhesive to complete the modular assembly.

248. In addition, Hitachi has developed a microminiature multichip pin grid array module. This 45mmx45mm module (Fig 39) has 208 I/O pins. Unlike the RAM module just described, the PGA module uses a more conventional alumina ceramic base. However, it does use a 20 mm square mother chip to interconnect CMOS gate arrays in a "silicon-on-silicon" arrangement. Flip chip reflow soldering and a silicone protective gel are also used.

Telecommunication Applications

249. A new packaging technology is being developed at AT&T Bell Laboratories. This microminiature multichip module technology, which is referred to as advanced VLSI packaging (AVP), is



MICROMINIATURE PIN-GRID ARRAY MULTICHIP MODULE

FIGURE - 39

designed to meet the needs of future VLSI based telecommunications and data processing systems. It is expected that these systems will incoroporate the use of mixed device technologies, for instance, MOS and bipolar, silicon and gallium arsenide.

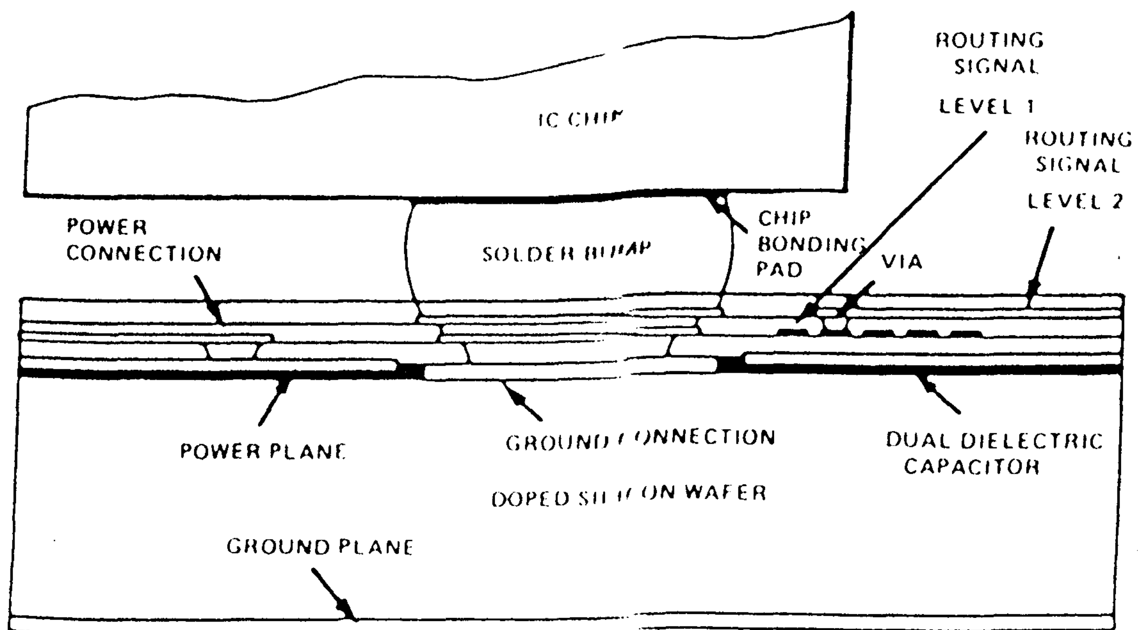
250. The AVP interconnection substrate is constructed to provide an excellent environment in whicfh to route signal paths and distribute voltage reference levels. The substrate provides a microstrip configurations for two signal levels over a continious power plane that acts as a high frequency ground, as shown in Fig 40.

251. The metallization of both signal lines and voltage planes is plated copper. The use of copper assures flexibility in altering line thickness and thus provides line resistivity values as designs require.

252. Good electrical contact between interconnection levels is achieved with solid nickel vias that are also plated. Signal level "microvias" measure 10 micro meter (o.4mil) in diameter, and power/ground vias measure 90 micrometer in diameter.

253. Polyimide forms the dielectric between metallized levels. characteristic impedances of 50 to 70 ohm can be achieved with dielectric thicknesses of 6 to 10 micro meter with line widths and spacings of 10 micrometer.

254. The use of AVP technology enables the extension of the high level of integration of VLSI integrated circuits to the system level by allowing as many as 100 comples VLSI chips to be



CROSS SECTION OF AVP MULTICHIP MODULE

FIGURE - 40

interconnected on a single silicon wafer. This ability to place large scale systems or subsystems or on AVP silicon wafers leads to minimal electrical parasitics, which, in turn, results in higher system operating frequencies and lower power dissipation.

255. Signal nets on multilayer boards may easily exceed 500 mm in total length, while nets and AVP substrates rarely exceed 100mm. Thus, output driver circuits typically have to drive board levels loads of more than 100pf, whereas most interconnection paths for AVP circuits require drivers designed for only 25pf loading. In addition, flip-chip solder bump attachment removes the need to route interanally generated signals to the perimeter of the chip, resulting in minimal integrated circuit parasitics.

256. What this leads to is that, by tailoring the size of the CMOS driver to the load, the total delay through the circuit is reduced about 50%. A large part of this delay reduction is accounted for within the smaller driver circuit.

257. Power dissipation levels are also reduced by shortening interconnection lengths and reducing capacitive loading. For high I/O VLSI desings, output drivers can account for up to 40% of the total chip power dissipation. By reducing the capacitive loading by a factor of up to 4, total chip power can be reduced by up to 30%.

258. The first implementation of the AVP module was a three chip laboratory test vehicle consisting of a central processing chip, a memory mangement chip, and a math accelerator chip. The chip I/Os range from 81 to 120. The 13mmx30mm silicon interconnection

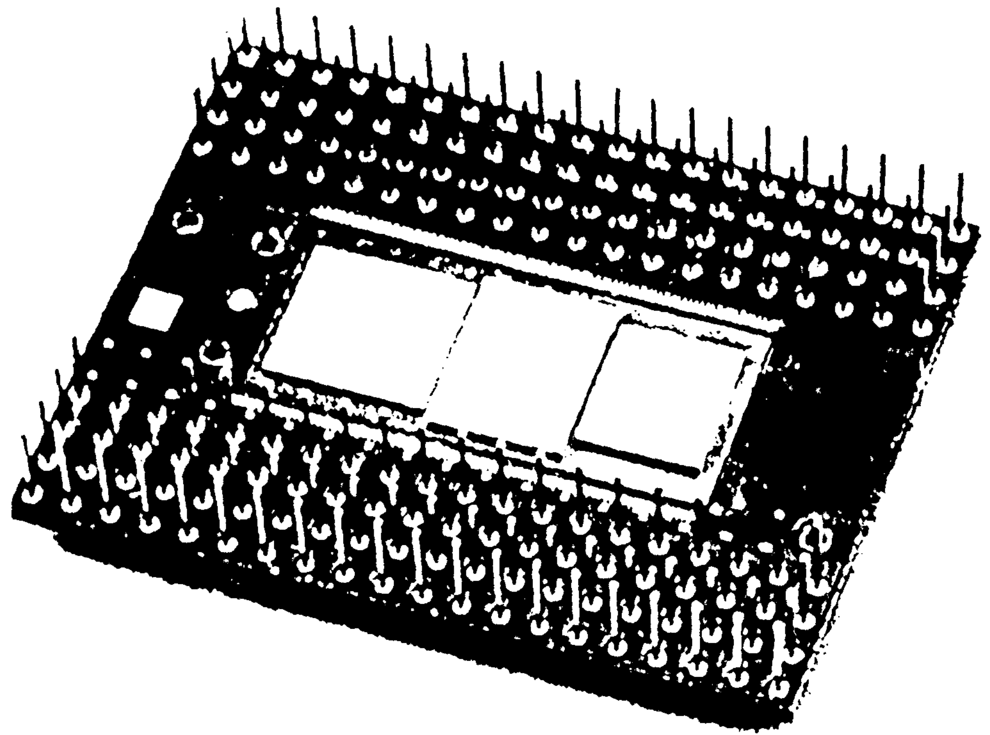
substrate within the module is not much larger than the chips themselves.

259. The chips are spaced 0.5mm apart, with most of the conductor routing taking place under the chips. Given abundant routing area, signal paths were widened to 20 micrometer, and all signal nets were brought to the periphery of the wafer for full test access.

260. The complete multichip module (Fig 41) is in the form of a 160 I/O pin grid array package with a four layer printed wiring board overall substrate with minimum design features of 0.1mm lines and 0.15 mm spaces. The board is fabricated using bismaleimide triazine (BT) epoxy blends to accommodate thermosonic wire bonding at 150°C.

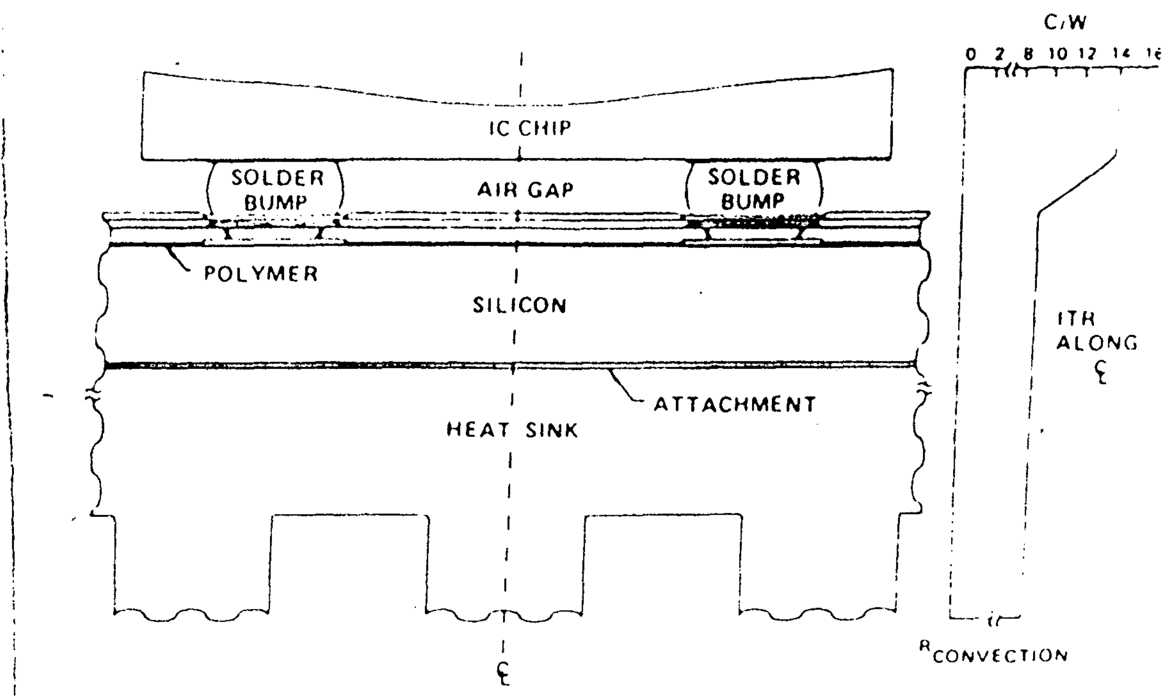
261. A rectangular cutout is routed in the center of the package to provide space for a metal heat sink/structural support member. The AVP interconnect substrate with the three chips flip-cgips mounted is assembled to the aluminum heat sink using a thin layer of compliant silicone gel adhesive (Fig 42).

262. The heat sink structure is assembled to the printed wiring board and assembly is then thermosonically ball/wedge bonded using 0.001 in. diameter gold wire. A protective plastic cover, designed with alignment tabs, provides the final mechanical protection for lthe wire bonded assembly.



THREE CHIP AVP MODULE WITHOUT PROTECTIVE COVER

FIGURE-41.



INTERNAL THERMAL RESISTANCE OF AVP MODULE

FIGURE - 42

Command Control Communication Applications

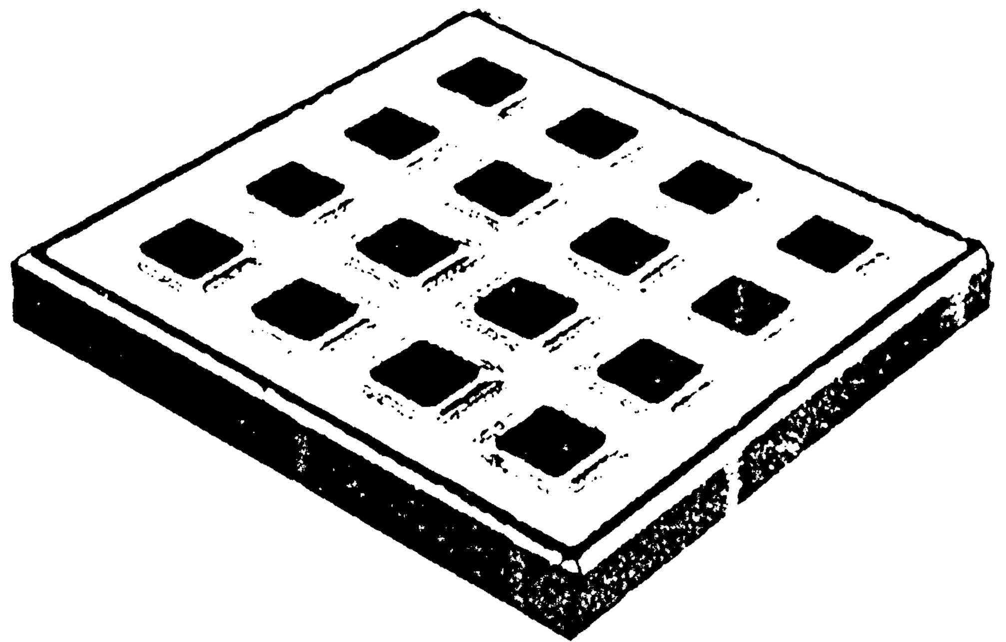
263. In the realm of command control communicate, primarily military application, the success of the mission is of prime importance. Therefore, companies trying to satisfy c-3 requirements have a slightly different viewpoint as to what is cost-effective compared to the commercial computer and tele-communication applications just described. However, as the following technology description will show, ther are not nearly as many differences in end results as one might expect.

264. IBM Federal Systems Division Multichip Modules. A micro-miniature 500,000 gate multichip package (MCP) is being offered by IBM for next generation c-3 applications for use with 50MHz CMOS integrated circuits that have features sizes as small as 0.5 micro meter. The 64 mm square MCP module (Fig 43) will have a cofired multilayer ceramic substrate that will accomodate 16 chip sites.

265. Each module will have 236 signal I/Os. The overall module itself will have 625 I/O pins on 2.54mm centers, including 498 I/Os for signals.

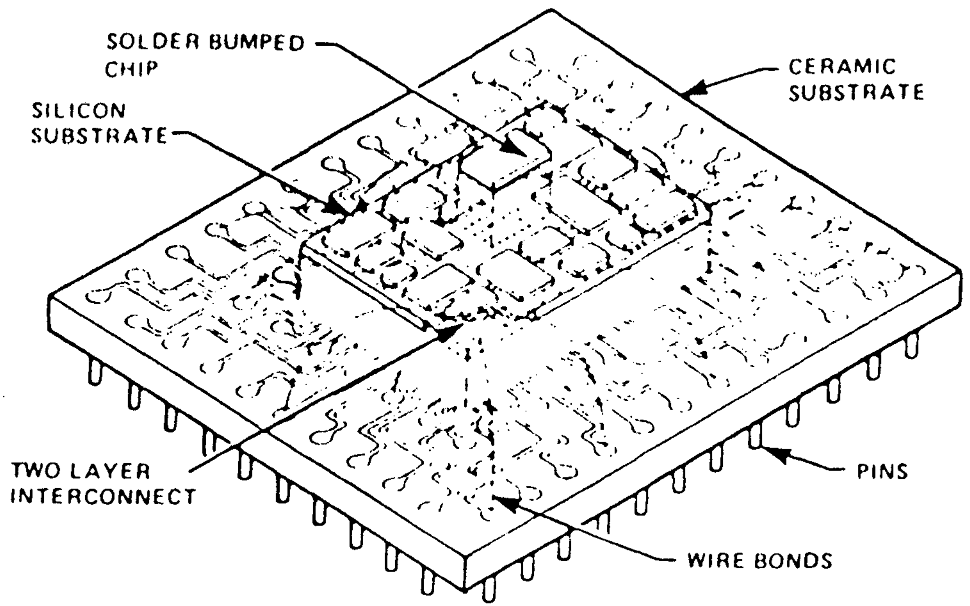
266. Package heremeticity will be established by using a ceramic cap, which is reflow solder sealed to the substrate. Maximum power for the package is expected to be less than 30W, with a 3 W maximum power for each chip.

267. Honeywell Bull Multichip Modules. Honeywell Bull has developed a "silicon on silicon" multichip module concept for



MCP MULTICHIP MODULE

FIGURE - 43



SILICON ON SILICON MODULE

FIGURE - 44

both C-3 and computer applications. The concept (Fig 44) combines flip-chips, a silicon substrate, a ceramic package or header, and conventional wire bonding or copper polyimide beam tape automated bonding between the silicon substrate and the package.

268. Low cost packaging can be achieved, since the silicon substrate utilizes conventional integrated circuit fabrication processses and materials. Silicon substrate quality is not critical when active devices are not present in the interconnection substrate.

269. Microminiature multichip packaging of this type also yields high density interconnects. Using flip chip technology, the chips can be placed relatively close together.

270. Another benefit of silicon on silicon packaging is repairability. The solder bumping and assembly processes can be repeated if chips have to be repaired or replaced. Also, since the integrated circuits are fabricated independently from the silicon substratae, it is possible, if not highly desirable, to mix chip technologies in the same module.

271. <u>Related Technologies</u>. The work being done by original equipment manufacturers to package multichip modules use, for the most part, existing fabrication and assembly technologies. However, work is also being done by independent supliers to develop more sophisticated interconnecting structures for these applications. Some of the most promising of these interconnection technologies have been considered.

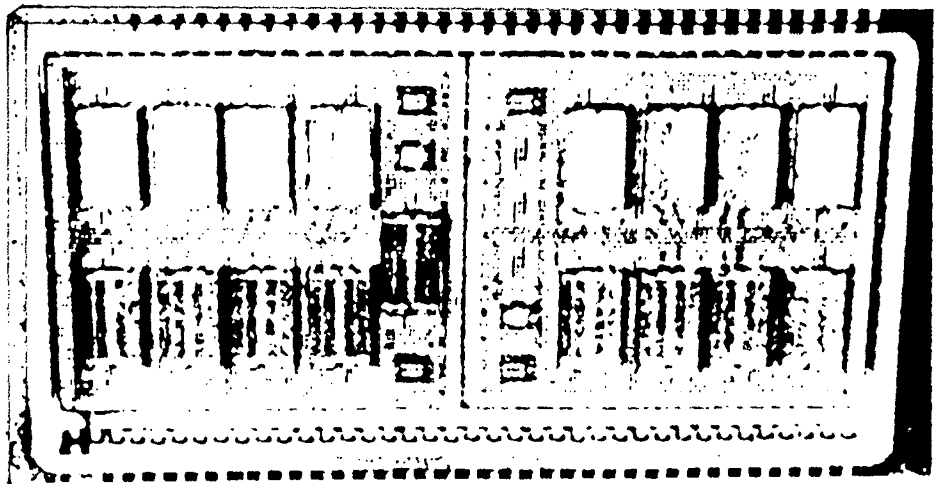
272. <u>Mosaic System Silicon Circuit Boards</u>. The foundation for Mosaic systems new multichip module interconnection substrate is a high density silicon circuit board. The basic element of SCB is a "sea of bonding pads" vertically connected to a matrix of conducting lines separated at over 100.00 intersections by a electrically programmable amorphous silicon "antifuse".

273. To make an SCB, a metal layer is deposited on the silicon substrate, followed by a silicon dioxide dielectric layer, which in turn is followed by a additional metal layer. The two metal layers are vertically connected to 840 bonding pads distributed over the surface of the segment.

274. The "antifuses" between the intersections of the conductor lines are made of a material that normally has a high resistance. However, when a voltage above a certain threshold is applied, the material switches to a low resistance. This action is opposite to that of a fuse. Thus, it forms an overall interaconnection pattern by connecting the conductor lines at preprogrammed intersections.

275. The small, 0.3mm bond pitch permits the SCB to handle some relatively high padout die in a very small footprint. subsequent wire bonding interconnects the chips to the silicon circuit board.

276. Fig 45 shows two 25 mm square SCBs assembled together to hold a 1.1 Mbit SRAM. It is composed of seventeen 64Kx1SRAM integrated circuit chips plus six buffers to drive the memory.



A 1·1 MBIT SRAM SILICON CIRCUIT ASSEMBLY

FIGURE - 45

277. <u>**Raychem High Density Interconnect Technology**</u>. The Raychem Corporation has (San Jose, California) combined the use of integrated circuit manufacturing processes with specialty materials to make custom designs for multichip modules using thin film aluminum multilayer techniques. Called HDI, for high desity interconnects, the multichip module interconnection substrate has 25 micro meter lines and spaces. Fig 46 shows a partial close-up view of a four chip module.

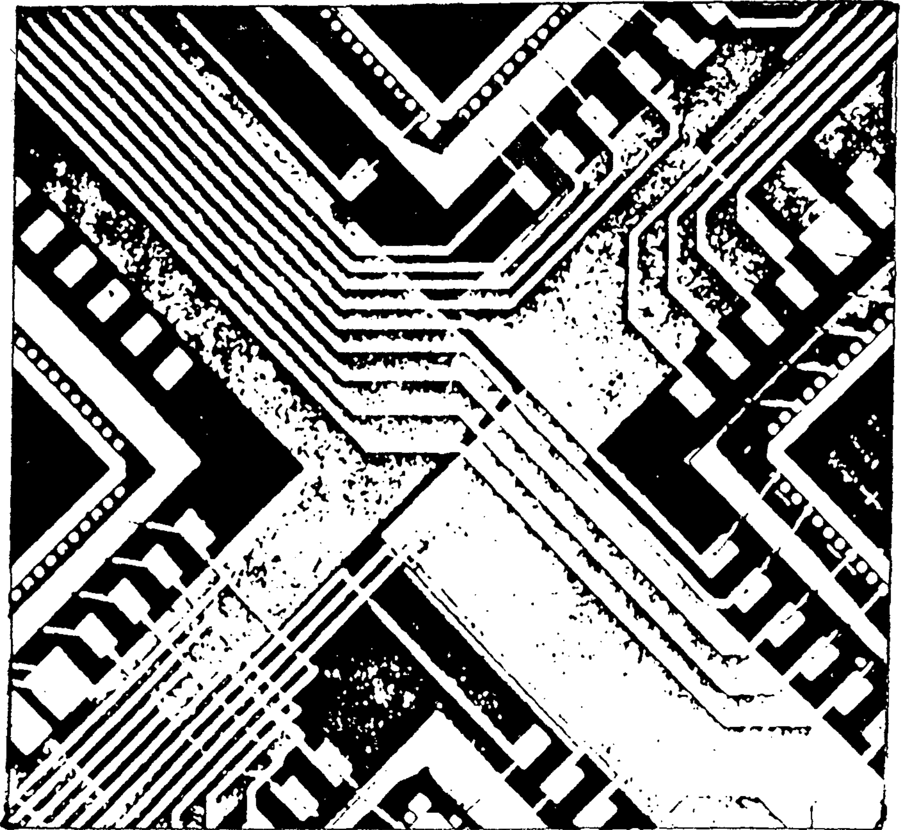
278. A cross section through the structure (Fig 47) shows HDI's special features. The conductors are 5 micrometer thick; the dielectric is 10 micrometer thick; and vias are 30 micro meter in diameter.

279. Significantly, the vias are not stacked one above the other. Rather, they are staggered, so that the one above is offset from the one below, either in a linear chain or in a spiral staircase. These staggered vias are considered by Raychem to be more robust to thermal cycling than stacked vias.

280. Designs with up to five metal layers have been fabricated by alternating aluminum metal conductor patterns with polyimide dielectric on a ceramic base substrate. Power and ground planes can be fabricated where needed for controlled impedance orfor low coupling noise on signal traces.

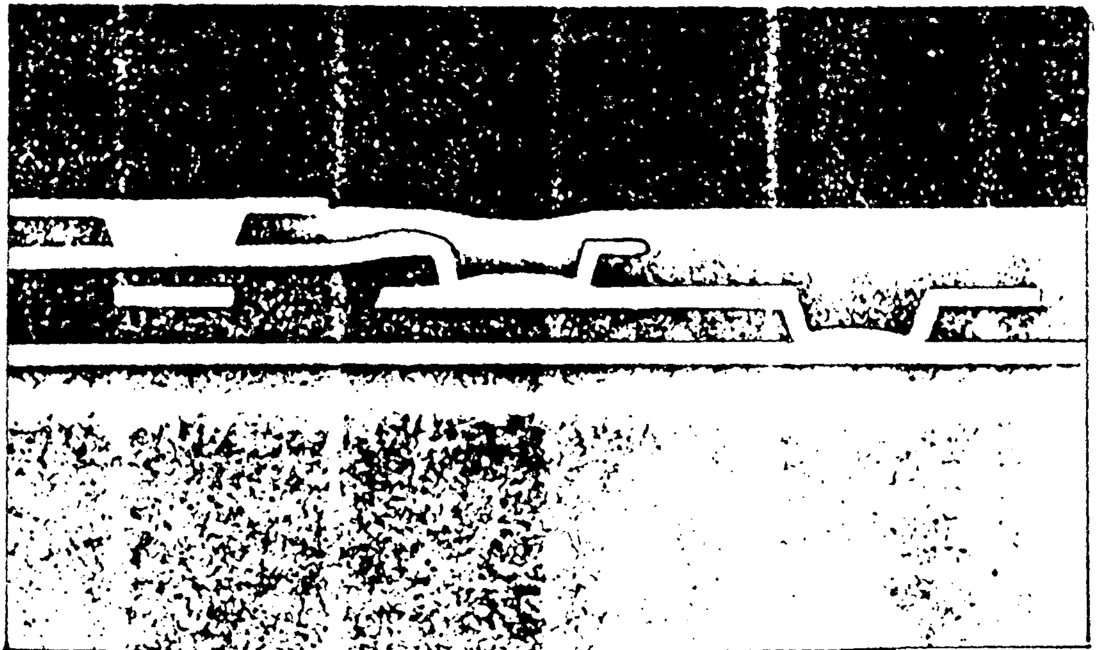
<u>**Advanced Water Scale packaging**</u>

281. The quest continues for a practical way to put entire systems on a single wafer, even though earlier attempts at wafer



CLOSE UP VIEW OF HIGH DENSITY INTERCONNECT TECHNOLOGY

FIGURE - 46



CROSS SECTION OF HDI TECHNOLOGY

FIGURE - 47

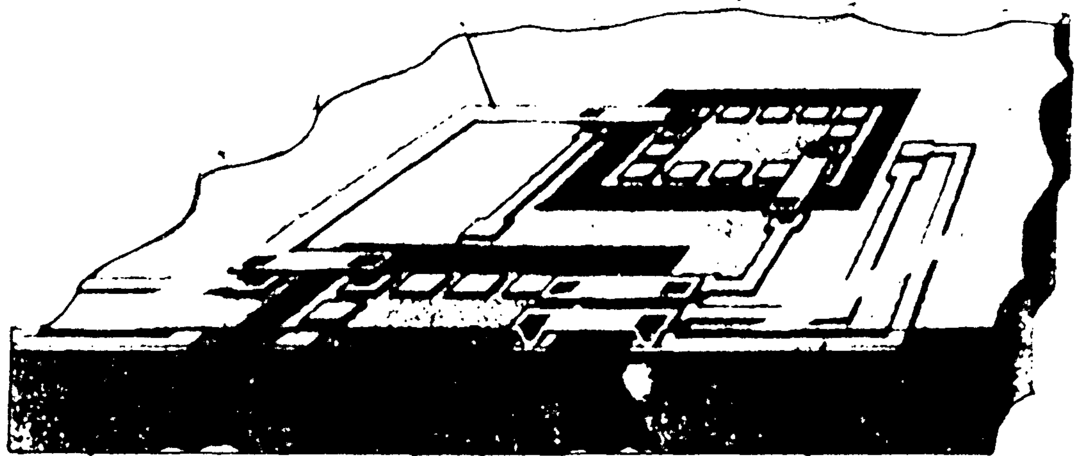
scale integration were plagued by intractable problems with yield and discretionary wiring. To date the approaches taken by Rockwell International and Mosaic systems represent the closest attempts to achieve full WSI. However, packaging engineers are not giving up, because systgem performance now depends as much on the connections between the integrated circuit chips as it does on what goes on in the chips themselves.

Auburn University Planar Hybrid Interconnection Technology.

282. Research scientists at the Microelectronics Science and Technology Centre of Auburn University are developing a silicon-base, hybrid wafer scale packaging technology that they say promises to solve WSI problems. Although their interconnection concept (Fig 48) uses a silicon wafer as the master interconnection medium, the semiconductor chips are not mounted on its surface. Instead, they are placed into the wafer.

283. The process steps begin with chemically etching rectangular cutouts (holes) into the silicon wafer and having interchip metallization paths deposited and patterned on its surface. Pretested chips are then mounted in the holes with their top surface coplanar with the wafer's surface. Electrical connection from chip to wafer is made by either wire bonding or with thin film metal links.

284. **Rensselaer Polytechnic Institute Wafer Transmission Module.** Recently, research efforts at Rensselaer Polytechnic Institute have been directed towards developing cost-effective, multilayer metal polyimide structurers for use with gallium arsenide (GaAs)



PLANAR HYBRID INTERCONNECTION TECHNOLOGY

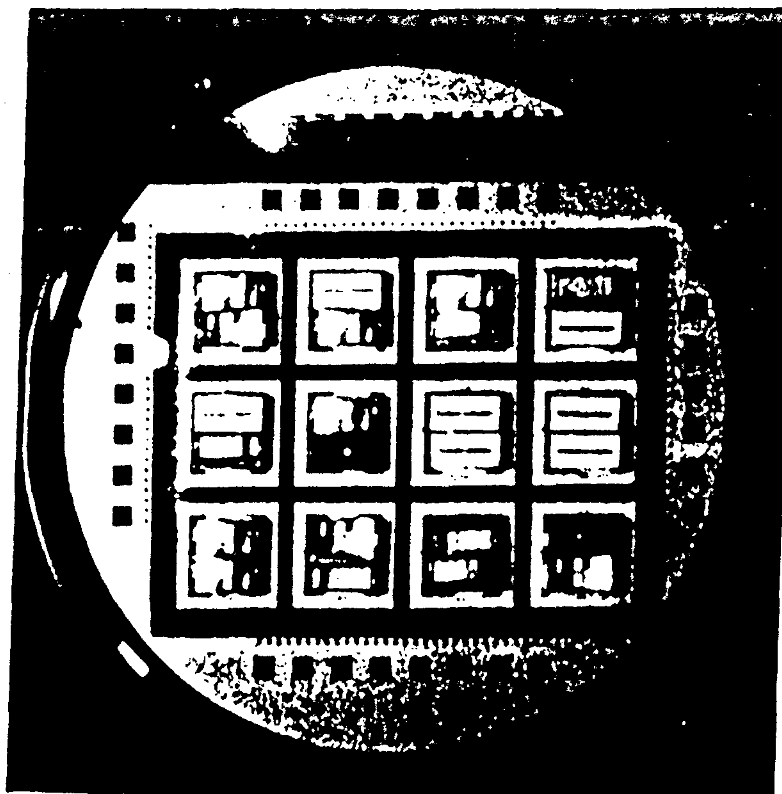
FIGURE - 48

devices at a wiring pitch of only a few micrometers. An advantage of this approach, which is variously termed as the wafer transmission module (WTM) or the wafer scale hybrid (WSH), is that all the wiring capacitance can be made small as a result of the low dielectric constant of polyimide.

285. Fig 49 shows a prototype of the wafer transmission module, with a fully developed WTM bonding technology, the die spacing could be made extremely tight, resulting in a effective gate density approximating that of an ultralarge scale integraed (ULSI) circuit.

286. The resulting multilayer structure resembles a minimaturized printed circuit board, with integrated circuit chips and other components bonded directly to the surface. such a hybrid package can also beregarded as supplying the additional layers of interconnections needed to improve the active device density to better exploit the speed of gallium arsenide devices.

287. Unfortunately, the yield of GaAs is currently so low that utilizing the maximum achievable device density is extraordinarily expensive. Hence, until the yield/cost problems associated with this approach are solved, the more traditional microminiature multichip module packaging schemes will be more attrative alternatives.



WAFER TRANSMISSION MODULE PROTOTYPE

FIGURE - 49

CONCLUSION

288. Through this study an endeavour has een made to give an insight into various Surface Mount and other related technologies that are under active development throughout the electronics industry. While the focus has been primarily on the hardware aspects of surface mounting implementation, many other disciplines have also been covered.

289. The potentials of using chip carriers and other surface mounted components are great (Table 16). Yet there exist some critical problems to be solved in successful applications. Key among these are the following :-

(a) Thermal Mamgement. Involving both the thermal expansion mismatch at the component/substrate level and the overal dissipation of heat at the system level.

(b) Electrical Performance. With respect to achieving the high circuit performance of the VLSI components without undue degradation caused by the packaging and interconnecting structure.

(c) Cost-Effective Fabrication. In conjunction with the development of new fabrication, assembly, and testing concepts and equipment.

290. The following points can be made about electronic packaging in general, and surface mounting in particular :-

Characteristics	Through-hole	Leaded surface mount	Leadless surface mount	Direct deposit	Bare chip
Packaging density	Low	Moderate	Good	Good	High
Standardization	Very good	Good	Good	Good	Limited
Thermal performance	Moderate	Good	Very good	Good	Fair
Substrate choices	Very good	Very good	Good	Fair	Limited
Fab investment	Low	Low	Moderate	Moderate	High
Assembly investment	Moderate	Low	Moderate	Moderate	High
Support investment	Low	Moderate	Moderate	High	High
External assembly services	Very high	High	Moderate	Moderate	Limited
Maintenance skills	Low	Moderate	Moderate	High	High
Change risk	Very low	Low	Moderate	Moderate	High
Assembly test	Very easy	Easy	Moderate	Moderate	Complex
Documentation	Easy	Easy	Moderate	Complex	Complex
Logistics support	Field change	Field change	Field change	Field change	Factory only
Inspect (circuit)	100% test	100% test	100% test	100% test	Lot accept
Component burn-in	Easy	Easy	Easy	Easy	Impractical
Pretest	Very easy	Very easy	Easy	Easy	Impractical
Change and repair	Easy	Easy	Easy	Easy	Difficult
Chip availability	Excellent	Very good	Good	Good	Limited
Multiple sourcing	Excellent	Very good	Good	Good	Limited
Footprint commonality	Excellent	Very good	Good	Good	Poor
Profile	High	High	Moderate	Low	Low

TABLE -16 A COMPARISON OF INTEGRATED CCT PACKAGING TECHNOLOGY

(a) Although new, high density, discrete packaged component technologies, such as multichip modules, are gaining importance, they do not represent a long term solutions for VLSI and ULSI applications.

(b) New multichip (and surface mount) packaging technologies can be successfully introduced into products only if equivalent progress is made on the associated system technologies, including design, interconnection, assembly, and testing.

(c) As the breadth of applications of VLSI based electronics increses, so will the diversity of packaging designs and technologies.

(d) Packaging development activity is rapidly extending beyond the needs of VLSI. New device techcnologies, for instance, gallium arsenide, optical interconnects, and cryogenic operating temperatures, are imposing new requirements on package design and technology.

291. The extent to which surface mounting will be used in future VLSI based products will depend on both the performance gains that can be achieved and the costs. However, a cost effective technology will not guarantee a successful introduction of surface mounting into system designs. When companies develop the needed infrastructure to meet these challenges successfully, the electronics industry will take a major step toward the fabrication of more sophisticated electronics equipment.

BIBLIOGRAPHY

1. Electronic Magnetic and Thermal Properties of Solid Materials - Klaus Schroder.

2. Magnetic Bubble Memory Technology - Hsu Chang.

3. End User's Guide to Innovative Flexible Circuit Packaging - Jay J Miniet.

4. Surface Mount and Related Technology - Gerald Ginsberg.

REMARKS BY GUIDE

REMARKS BY EXTERNAL EXAMINER

REMARKS BY DEAN